LITTLE FOOT®

Surface-Mount Power MOSFETs
Featured Products

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About LITTLE FOOT® Power MOSFETs

LITTLE FOOT power MOSFETs are being designed into computer and computer peripheral products, telecom systems, automotive air bags, and numerous other applications where space-savings and efficiency are at a premium. Built on high-density trench and low-threshold planar technologies, LITTLE FOOT leads the industry for low-voltage, surface-mount power MOSFET performance.

TEMIC has expanded the scope of the LITTLE FOOT family beyond the classic SO-8 to include devices in the TSSOP-8*, TSSOP-28, and TSOP-6 packages, giving you even more genuine LITTLE FOOT options for your designs. Whether your application is load switching, power switching, dc-to-dc conversion, battery switching, or motor control, there's a LITTLE FOOT device that can help you reduce component count, save space, and use power more efficiently.

This publication includes complete data sheets for all the latest generations of LITTLE FOOT devices. To obtain data sheets for older members of the LITTLE FOOT family, please visit our web site at http://www.temic.com. Data sheets for all LITTLE FOOT products are also available from our faxback system using the document numbers provided in the LITTLE FOOT selector guide, which begins on page *i* of this data book.

About TEMIC Semiconductors

TEMIC Semiconductors is a division of TEMIC, a Daimler-Benz microelectronics company. Member of TEMIC Semiconductors include Siliconix, Telefunken Semiconductors, Matra MHS, and Dialog Semiconductors. With a rich technology portfolio including bipolar, CMOS, DMOS, silicon germanium and RF bipolar processes, TEMIC Semiconductors provides solutions that save space, prolong battery life, and reduce component count in pacesetting microelectronic designs.

* Formerly known as LITE FOOT®.

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Selector Guides

TSOP-6 (N-Channel)

Part Number	Maximum Ratings					Page or FaxBack Number
	V_{DS} (V)	$r_{DS(on)}$ (Ω)			I_D (A)	
		V_{GS} = 10 V	V_{GS} = 4.5 V	V_{GS} = 2.5 V		
Si3442DV	20		0.070	0.095	±4.0	1-11
Si3454DV	30	0.065	0.095		±4.2	1-15
The following products are currently in development and are scheduled for release in Q1-Q2, 1997.						
Si3445DV	20		0.035	0.060		
Si3456DV	30	0.035	0.060			

TSOP-6 (P-Channel)

Part Number	Maximum Ratings					Page or FaxBack Number
	V_{DS} (V)	$r_{DS(on)}$ (Ω)			I_D (A)	
		V_{GS} = 10 V	V_{GS} = 4.5 V	V_{GS} = 2.5 V		
Si3441DV	20		0.100	0.135	±3.3	1-7
Si3455DV	30	0.100	0.190		±3.5	1-19
Si3457DV		0.065	0.100		±4.2	1-23
The following product is currently in development and is scheduled for release in Q1-Q2, 1997.						
Si3443DV	20		0.055	0.100		

TSSOP-8 (N-Channel)

Part Number	Maximum Ratings						Config.	Page or FaxBack Number
	V_{DS} (V)	$r_{DS(on)}$ (Ω)				I_D (A)		
		V_{GS} = 10 V	V_{GS} = 4.5 V	V_{GS} = 3.0 V	V_{GS} = 2.5 V			
Si6426DQ	20		0.035		0.040	±5.4	Single	70174[a]
Si6926DQ			0.035	0.040	0.045	±4.0	Dual	2-37
Si6925DQ			0.050	0.060	0.080	±3.4	Dual	2-33
Si6946DQ			0.080		0.110	±2.8	Dual	2-49
Si6956DQ		0.090	0.175			±2.5	Dual	70173[a]
Si6434DQ	30	0.028	0.042			±5.6	Single	2-9
Si6436DQ		0.045	0.070			±4.4	Single	70169[a]
Si6954DQ		0.065	0.095			±3.9	Dual	2-53
The following products are currently in development and are scheduled for release in Q1-Q2, 1997.								
Si6466DQ	20		0.014		0.021		Single	
Si6966DQ			0.035		0.050		Dual	
Si6410DQ	30	0.014	0.021				Single	
Si6926DQ		0.035	0.050				Dual	

Note
a. The data sheet for this product has not been included in this publication. It is available on the TEMIC web site (http://www.TEMIC.com) or via facsimile by calling Siliconix FaxBack, 1-408-970-5600 and requesting the FaxBack document number indicated.

TSSOP-8 (P-Channel)

Part Number	Maximum Ratings					Config.	Page or FaxBack Number
	V_{DS} (V)	$r_{DS(on)}$ (Ω)			I_D (A)		
		V_{GS} = –10 V	V_{GS} = –4.5 V	V_{GS} = –2.5 V			
Si6433DQ	–12		0.060	0.090	± 4.0	Single	2-5
Si6943DQ			0.100	0.180	± 2.5	Dual	2-45
Si6447DQ	–20	0.090	0.160		± 3.2	Single	70170[a]
Si6953DQ		0.170	0.320		± 1.9	Dual	70172[a]
Si6415DQ	–30	0.019	0.030		± 6.5	Single	2-1
Si6435DQ		0.040	0.070		± 4.5	Single	2-13
Si6933DQ		0.045	0.085		± 3.5	Dual	2-41
Si6955DQ		0.085	0.190		± 2.5	Dual	2-57
Si6459DQ	–60	0.120	0.150		± 2.6	Single	2-17
The following products are currently in development and are scheduled for release in Q1-Q2, 1997.							
Si6463DQ	–20		0.020	0.035		Single	
Si6963DQ			0.055	0.100		Dual	

TSSOP-8 (Complementary Devices)

Part Number	Maximum Ratings					Config.	Page or FaxBack Number
	V_{DS} (V)	$r_{DS(on)}$ (Ω)			I_D (A)		
		V_{GS} = ± 10 V	V_{GS} = ± 4.5 V	V_{GS} = ± 2.5 V			
Si6552DQ	20 –12		0.080 0.100	0.110 0.180	± 2.8 ± 2.5	N-Channel P-Channel	2-27
Si6542DQ	20 –20	0.090 0.170	0.175 0.320		± 2.5 ± 1.9	N-Channel P-Channel	70171[a]
Si6543DQ	30 –30	0.065 0.085	0.095 0.190		± 3.9 ± 2.5	N-Channel P-Channel	2-21
The following products are currently in development and are scheduled for release in Q1-Q2, 1997.							
Si6562DQ	20 –20	0.035 0.045	0.050 0.085			N-Channel P-Channel	
Si6544DQ	30 –30		0.035 0.055	0.050 0.100		N-Channel P-Channel	

TSSOP-28

Part Number	Maximum Ratings				Config.	Page or FaxBack Number
	V_{DS} (V)	$r_{DS(on)}$ (Ω)		I_D (A)		
		V_{GS} = 10 V	V_{GS} = 4.5 V			
N-Channel						
Si6331DQ	30	0.028	0.042	± 5.6	Triple	2-61
P-Channel						
Si6332DQ	–30	0.040	0.070	± 4.5	Triple	2-65
Triple Half-Bridge						
Si6361DQ	30 –30	0.065 0.085	0.095 0.190	± 3.9 ± 2.5	N-Channel P-Channel	2-69

Note
a. The data sheet for this product has not been included in this publication. It is available on the TEMIC web site (http://www.TEMIC.com) or via facsimile by calling Siliconix FaxBack, 1-408-970-5600 and requesting the FaxBack document number indicated.

8-Pin SOIC (N-Channel)

Part Number	Maximum Ratings						Config.	Page or FaxBack Number
	V_{DS} (V)	$r_{DS(on)}$ (Ω)				I_D (A)		
		V_{GS} = 10 V	V_{GS} = 6.0 V	V_{GS} = 4.5 V	V_{GS} = 2.5 V			
Si9426DY	20			0.0135	0.016	± 10	Single	3-89
Si9925DY				0.050	0.080	± 5.0	Dual	3-99
Si9926DY				0.030	0.040	± 6.0	Dual	3-103
Si9956DY		0.100		0.200		± 3.5	Dual	70140[a]
Si4420DY	30	0.009		0.013		± 12.5	Single	3-9
Si4410DY		0.0135		0.020		± 10	Single	3-1
Si4412DY		0.028		0.042		± 7.0	Single	3-5
Si9410DY		0.030		0.050		± 7.0	Single	70122[a]
Si4936DY		0.037		0.055		± 5.8	Dual	3-61
Si9936DY		0.050		0.080		± 5.0	Dual	70128[a]
Si4902DY		0.065 Ch-1 0.028 Ch-2		0.095 Ch-1 0.042 Ch-2		± 3.0 Ch-1 ± 6.7 Ch-2	Asym. Dual	3-51
Si9940DY	50	0.050		0.070		± 5.3	Dual 16-Pin	70129[a]
Si9955DY		0.130		0.200		± 3.0	Dual	70139[a]
Si4450DY	60	0.024	0.030			± 7.5	Single	3-25
Si4946EY		0.055		0.075		± 4.5	Dual	3-65
Si9945DY		0.100		0.200		± 3.3	Dual	70133[a]
Si9959DY		0.300				± 2.0	Dual	70142[a]
Si4480DY	80	0.035	0.040			± 6.0	Single	3-29
Si4980DY		0.075	0.095			± 3.7	Dual	3-81
The following products are currently in development and are scheduled for release in Q1-Q2, 1997.								
Si4966DY	20			0.020	0.030		Dual	
Si4466DY				0.090	0.013		Single	
Si4920DY	30			0.020	0.030		Dual	

8-Pin SOIC (P-Channel)

Part Number	Maximum Ratings						Config.	Page or FaxBack Number
	V_{DS} (V)	$r_{DS(on)}$ (Ω)				I_D (A)		
		V_{GS} = –10 V	V_{GS} = –4.5 V	V_{GS} = –2.7 V	V_{GS} = –2.5 V			
Si9424DY	–12		0.025		0.033	± 7.7	Single	3-85
Si9434DY			0.040		0.060	± 6.4	Single	70147[a]
Si9934DY			0.050		0.074	± 5.0	Dual	3-107
Si9433DY	–20		0.065		0.100	± 5.4	Single	70125[a]
Si9933DY			0.110	0.190		± 3.4	Dual	70127[a]
Si9430DY		0.050	0.090			± 5.8	Single	70124[a]
Si9400DY		0.250	0.400			± 2.5	Single	70119[a]
Si9405DY		0.100	0.160			± 4.3	Single	70120[a]
Si9947DY		0.100	0.190			± 3.5	Dual	70134[a]
Si9953DY		0.250	0.400			± 2.3	Dual	70138[a]

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8-Pin SOIC (P-Channel)

Part Number	Maximum Ratings						Config.	Page or FaxBack Number
	V_{DS} (V)	$r_{DS(on)}$ (Ω)				I_D (A)		
		V_{GS} = –10 V	V_{GS} = –4.5 V	V_{GS} = –2.7 V	V_{GS} = –2.5 V			
Si4425DY		0.014	0.023			± 11	Single	3-13
Si4925DY		0.032	0.045			± 6.1	Dual	3-57
Si4435DY		0.020	0.035			± 8.0	Single	3-21
Si4431DY	–30	0.040	0.070			± 5.8	Single	3-17
Si4953DY		0.053	0.095			± 4.9	Dual	3-77
Si9435DY		0.055	0.105			± 5.1	Single	70126[a]
Si4947DY		0.085	0.190			± 3.5	Dual	3-69
Si4948EY		0.120	0.150			± 3.1	Dual	3-73
Si9407DY	–60	0.150	0.240			± 3.0	Single	70121[a]
Si9948DY		0.280	0.500			± 2.0	Dual	70135[a]
The following products are currently in development and are scheduled for release in Q1-Q2, 1997.								
Si4463DY	–20		0.014		0.020		Single	
Si4963DY			0.030		0.050		Dual	

8-Pin SOIC (Complementary Devices)

Part Number	Maximum Ratings						Config.	Page or FaxBack Number
	V_{DS} (V)	$r_{DS(on)}$ (Ω)				I_D (A)		
		V_{GS} = ± 10 V	V_{GS} = ± 4.5 V	V_{GS} = ± 2.7 V	V_{GS} = ± 2.5 V			
Si9529DY	20 –12		0.030 0.050		0.040 0.074	± 6.0 ± 5.2	N-Channel P-Channel	3-99
Si9928DY			0.050 0.110	0.080 0.190		± 5.0 ± 3.4	N-Channel P-Channel	70143[a]
Si9958DY	20 –20	0.100 0.100	0.150 0.190			± 3.5	N-Channel P-Channel	70141[a]
Si9942DY		0.125 0.200	0.250 0.350			± 3.0 ± 2.5	N-Channel P-Channel	70130[a]
Si9952DY	25 –25	0.100 0.250	0.150 0.400			± 3.5 ± 2.3	N-Channel P-Channel	70137[a]
Si4539DY		0.037 0.053	0.055 0.095			± 5.8 ± 4.9	N-Channel P-Channel	3-39
Si9939DY	30 –30	0.050 0.100	0.080 0.160			± 3.5 ± 3.5	N-Channel P-Channel	70146[a]
Si4532DY		0.065 0.085	0.095 0.190			± 3.9 ± 2.5	N-Channel P-Channel	3-33
Si4559EY	60 –60	0.055 0.120	0.075 0.150			± 4.5 ± 3.1	N-Channel P-Channel	3-45
The following products are currently in development and are scheduled for release in Q1-Q2, 1997.								
Si4562DY	20 –20		0.020 0.030		0.030 0.050		N-Channel P-Channel	
Si4532DY	30 –30	0.020 0.030	0.030 0.050				N-Channel P-Channel	

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High-Efficiency, PWM Optimized MOSFETs

Part Number	Maximum Ratings				Config.	Package	Page or FaxBack Number
	V_{DS} (V)	$r_{DS(on)}$ (Ω) V_{GS} = 4.5 V	$r_{DS(on)}$ (Ω) V_{GS} = 3.0 V	I_D (A)			
Si9804DY	20	0.023	0.030	± 7.8	Single N-Channel	SOIC-8	4-27
Si9803DY	-20	0.040	0.060	± 5.9	Single P-Channel	SOIC-8	4-23
Si9802DY	20	0.055	0.075	± 4.5	Dual N-Channel	SOIC-8	4-19
Si9801DY	20 -20	0.055 0.080	0.075 0.120	± 4.5 ± 4.0	N-Channel P-Channel	SOIC-8	4-13
Si6802DQ	20	0.075	0.110	± 3.3	Single N-Channel	TSSOP-8	4-9
Si6801DQ	20 -20	0.160 0.190	0.260 0.280	± 1.9 ± 1.7	N-Channel P-Channel	TSSOP-8	4-3

Selector Guides

Note
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Selector Guide

TSOP-6 **1**

High-Efficiency, PWM Optimized MOSFETs

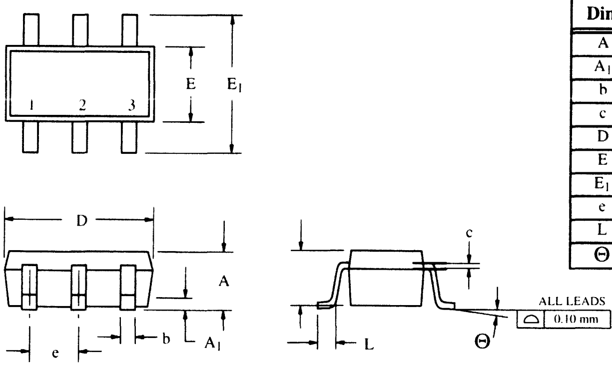
Appendix

Worldwide Sales Offices and Distributors

TSOP-6—The Next Step for LITTLE FOOT®

Cellular telephones, notebook computers, and other portable electronic systems are becoming smaller with each new generation of products. The new TSOP-6 LITTLE FOOT family anticipates this evolution. Its small size allows the placement of a MOSFET in spaces that have become too small for any other surface-mount power MOSFET package.

With a power rating of 2 W, on-resistance as low as 0.065 Ω, and current ratings of up to 4.2 A, the new LITTLE FOOT TSOP-6 (Figure 1) is a true power package, providing the kind of performance, on an even smaller scale, that designers have come to expect from LITTLE FOOT.



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	–	1.10	–	0.043
A_1	0.01	0.10	0.0004	0.004
b	0.25	0.50	0.010	0.020
c	0.10	0.26	0.004	0.010
D	2.90	3.10	0.114	0.122
E	1.30	1.70	0.051	0.067
E_1	2.75 BSC		0.108 BSC	
e	1.00 BSC		0.039 BSC	
L	0.20	0.60	0.008	0.024
Θ	0°	8°	0°	8°

Figure 1. TSOP-6 Outline Drawing

Not only is the TSOP-6 small, it's also a JEDEC registered package [with the same footprint as the SC-59, but with a lower profile and higher power rating (up to 2 W)]. As further assurance that the TSOP-6 will be established as the industry standard for low-voltage applications with limited circuit board space, these devices are being second-sourced by Motorola Semiconductors. For these TSOP-6 devices, Siliconix and Motorola have agreed on compatible pin-outs, power ratings, and package outlines and dimensions.

A New Branch of a Great Family

When Siliconix created the first true surface-mount power MOSFETs with its SO-8 LITTLE FOOT family, two innovations were involved: a lower on-resistance power MOSFET technology and modifications to the standard, surface-mount SOIC package. The lower on-resistance MOSFET reduced the power dissipation per unit of current, while the innovative packing provided a path for heat to escape, allowing high currents to be switched in a package that is much smaller and easier to assemble.

The introduction of LITTLE FOOT MOSFETs in the SO-8 inevitably raised the expectations of the market as regards surface-mounted power MOSFETs, resulting in a demand for devices with greater capabilities in even smaller packages. In 1994, Siliconix halved the size of the smallest available power MOSFET package with the introduction of the LITTLE FOOT TSSOP-8.

With the introduction of LITTLE FOOT devices in the TSOP-6, Siliconix is answering the demand of the market for smaller size and greater capabilities with even smaller devices that can provide the current handling available until now only in the TSSOP-8, SO-8, and other larger packages.

The Footprint

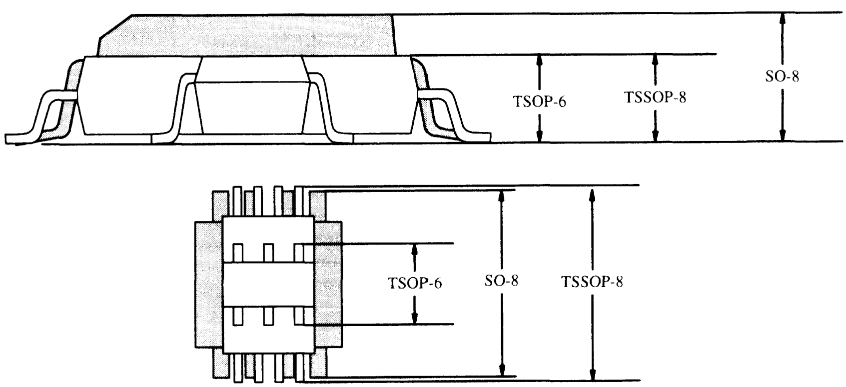


Figure 2. LITTLE FOOT® Family Package Evolution

The TSOP-6 is a 6-leaded, 1-mm thick package with a total height of 1.1 mm. The package and leads occupy an area of 2.75 × 3.10 mm. To put this in perspective, Figure 2 gives a visual comparison by overlaying the package outlines of the TSOP-6, the TSSOP-8 and the SO-8 packages. The TSOP-6 measures 2.75 mm in width, including the leads, less than half as wide as the SO-8. Table 1 gives a comparison of the dimensions of these packages.

Table 1. Comparison of Dimensions

Dim	TSOP-6				TSSOP-8				SOIC-8			
	Millimeters		Inches		Millimeters		Inches		Millimeters		Inches	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
Height	–	1.10	–	0.043	1.05	1.20	0.041	0.047	1.35	1.75	0.053	0.069
Lead Width	0.25	0.50	0.010	0.020	0.25	0.30	0.010	0.012	0.35	0.45	0.014	0.018
Package Length	2.90	3.10	0.114	0.122	2.90	3.10	0.114	0.122	4.69	5.00	0.185	0.196
Package Width	1.30	1.70	0.051	0.067	4.30	4.50	0.170	0.177	3.50	4.05	0.140	0.160
Width of Foot Print	2.75 BSC		0.108 BSC		6.20	6.60	0.244	0.260	5.70	6.30	0.224	0.248
Lead Pitch	1.00 BSC		0.039 BSC		0.65 BSC		0.025 BSC		1.27 BSC		0.050 BSC	

Thermal Capabilities

The same copper lead frame innovations introduced in the SO-8 LITTLE FOOT have been used in the TSOP-6 LITTLE FOOT to dissipate heat. The TSOP-6 lead frame is shown in Figure 3. As in the SO-8 and TSSOP-8 packages, the thermal path runs from the die, through the die attach, into the copper lead frame, and out the drain leads (Figure 4). The drain leads account for the largest portion of the thermal impedance due to the small cross sectional area of the leads. The small size of the package helps to keep the length of the drain leads short. The short lead length, in combination with the use of four drain leads, keeps the thermal impedance low for this size package.

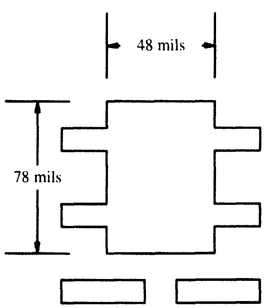


Figure 3. TSOP-6 Leadframe

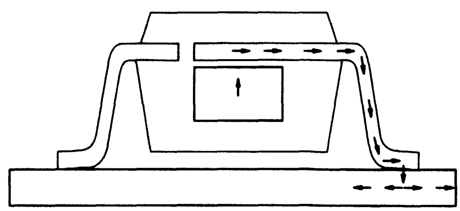


Figure 4. Thermal Path

The thermal rating as provided on data sheets for surface-mount MOSFETs is measured with the part mounted on a one-inch square piece of 0.062-inch thick FR4 PC board. This choice of test board is neither a "worst-case" or "best-case" layout. It represents a compromise between single-layer and multilayer boards, with more copper on its single side than the average single-layer construction. Thus, it can serve as an approximation of multilayer boards with center power planes and far less surface copper.

The junction is heated by a known amount of power for a known amount of time. The junction temperature is measured immediately after heating using the temperature coefficient of the forward voltage of the internal diode. This procedure is repeated from a time of 5 ms out to several hundred seconds. This series of measurements and measurement of the ambient temperature provides Rθja, the single pulse power curve, and provides the data required to generate the transient thermal impedance curves from junction to ambient.

Two Versions: 0.5 W and 2 W

Each TSOP-6 LITTLE FOOT device is available in two versions with different thermal ratings. The rating is dependent on the lead frame material used. The parts with the "V" suffix are built with a copper leadframe which gives the best thermal performance. The parts with the "X" suffix have an Alloy 42 leadframe. Although the "X" series devices are rated with the same electrical resistance as the "V" series devices, they are specified at a reduced current level to compensate for their increased thermal impedance.*

The first thermal performance parameter that is normally seen is Rθja. This parameter gives a means of comparing the package capability before the PC board starts to have a significant effect. For the TSOP-6, the board is considered to dominate after 5 seconds. Rθja for the TSOP-6 is 62.5°C/W for the "V" parts and 90°C/W for the "X" parts. The "V" parts, which have the copper lead frame compare very favorably with 50°C/W for the single-die SO-8, 62.5°C/W for the dual-die SO-8.

A comparison of the single-pulse power curves (Figure 5) reveals the difference in the thermal mass of the TSOP-6 and the SO-8 die and lead frames and therefore in ability of these two packages to handle surge currents. The single-pulse power curve shows the amount of power it takes for a single pulse of fixed duration to raise the junction temperature from room temperature to 150°C. If extended below 10 ms, the curves would become asymptotic and converge, reflecting the limitations of the die alone. The opposite end of the curve reflects the limitations of the PC board upon which the device is mounted. The difference in thermal mass shows up in between. The reduced thermal mass of the TSOP-6 results in a significant but reduced capability in pulse duration, amounting to less than 5 seconds. It should be noted that the TSOP-6 can dissipate a 30-W pulse of 10-ms duration.

*Samples of "V"-series devices are available now. Samples of "X"-series devices will be available in November 1996. Please contact us then at 1 800-554-5565 (1 408 567-8220 outside the U.S. and Canada) to receive data sheets for these devices.

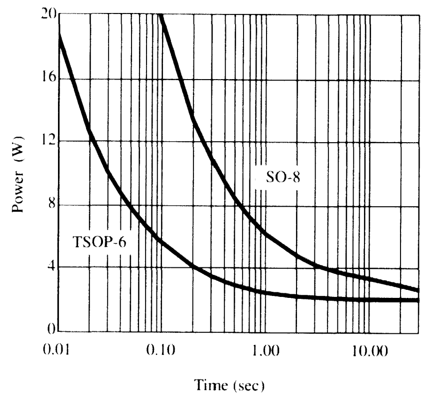


Figure 5. Single Pulse Power

The combination of very low on-resistance power MOSFET technology and a thermally efficient copper leadframe in the new LITTLE FOOT TSOP-6 package creates a new standard for performance per footprint. For applications requiring very low on-resistance, at less current, the Alloy 42-leadframes offer manufacturing advantages that make them even more economical.

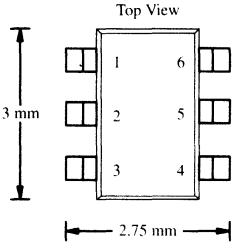
P-Channel Enhancement-Mode MOSFET

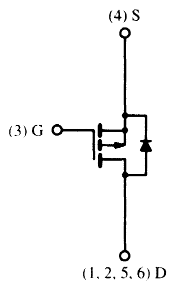
Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
–20	0.10 @ V_{GS} = –4.5 V	± 3.3
	0.135 @ V_{GS} = –2.5 V	± 2.9

2.5-V Rated

TSOP-6
Top View





P-Channel MOSFET

Power Dissipation

Si3441DV—2.0 W

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	–20	V
Gate-Source Voltage		V_{GS}	± 8	
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	± 3.3	A
	T_A = 70°C		± 2.6	
Pulsed Drain Current		I_{DM}	± 20	
Continuous Source Current (Diode Conduction)[a]		I_S	–1.6	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	2.0	W
	T_A = 70°C		1.28	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient[a]	R_{thJA}	62.5	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 5 sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70191.

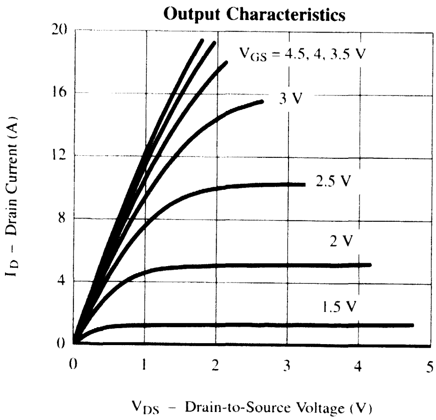
Specifications (T_J = 25°C Unless Otherwise Noted)

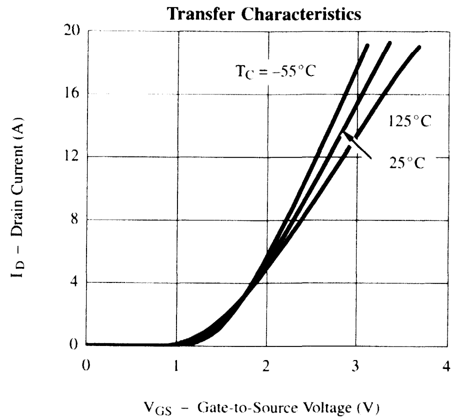
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 µA	–0.45			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±8 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = –20 V, V_{GS} = 0 V			–1	µA
		V_{DS} = –20 V, V_{GS} = 0 V, T_J = 70°C			–5	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} = –5 V, V_{GS} = –4.5 V	–10			A
		V_{DS} = –5 V, V_{GS} = –2.5 V	–4			
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = –4.5 V, I_D = 3.3 A		0.078	0.10	Ω
		V_{GS} = –2.5 V, I_D = 2.9 A		0.110	0.135	
Forward Transconductance[a]	g_{fs}	V_{DS} = –10 V, I_D = –3.3 A		8.8		S
Diode Forward Voltage[a]	V_{SD}	I_S = –1.6 A, V_{GS} = 0 V		0.8	–1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = –10 V, V_{GS} = –4.5 V, I_D = –3.3 A		8.6	14	nC
Gate-Source Charge	Q_{gs}			1.5		
Gate-Drain Charge	Q_{gd}			3.1		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = –10 V, R_L = 10 Ω I_D ≅ –1.6 A, V_{GEN} = –4.5 V, R_G = 6 Ω		27	50	ns
Rise Time	t_r			17	30	
Turn-Off Delay Time	$t_{d(off)}$			52	80	
Fall Time	t_f			45	70	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = –1.6 A, di/dt = 100 A/µs		50	80	

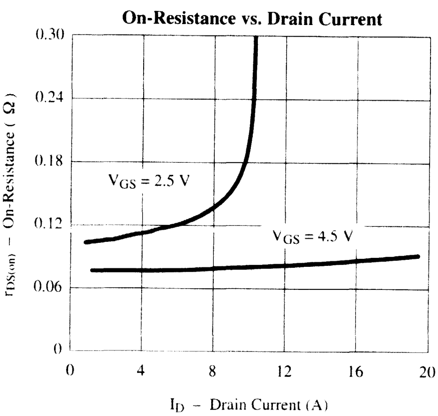
Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

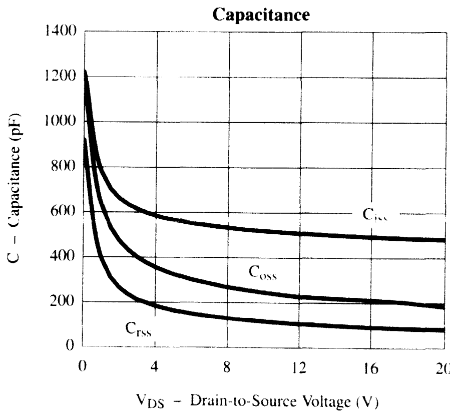
New Product

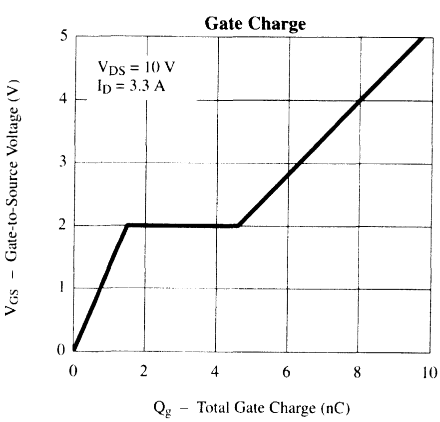
Typical Characteristics (25°C Unless Otherwise Noted)

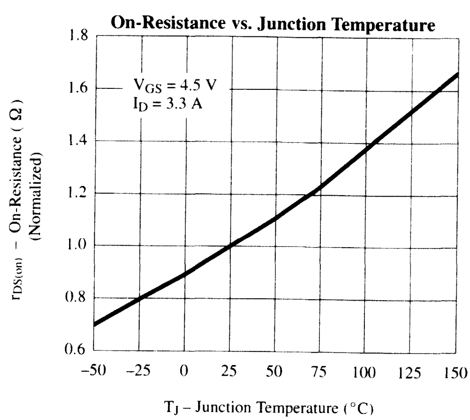












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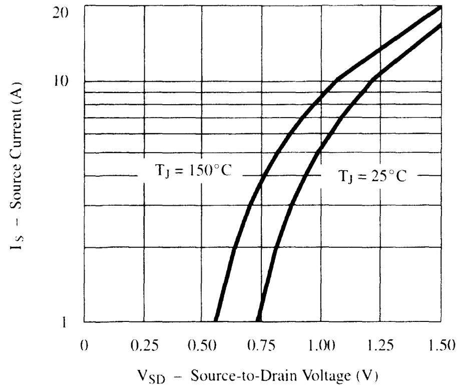
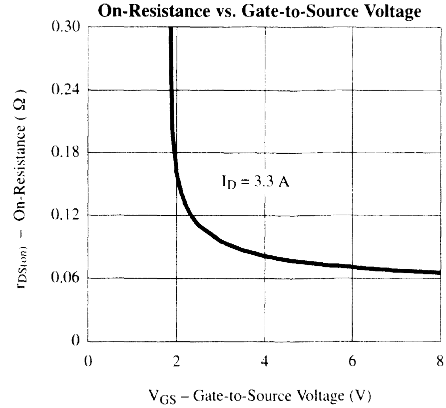
TSOP-6

Typical Characteristics (25°C Unless Otherwise Noted)

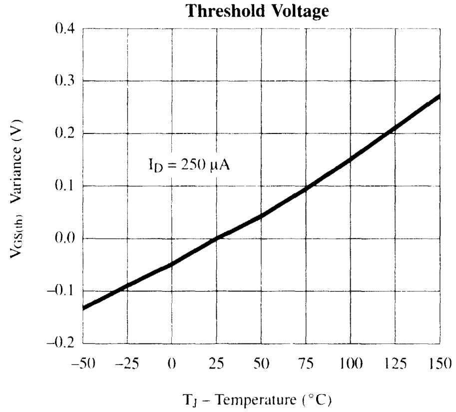
Source-Drain Diode Forward Voltage



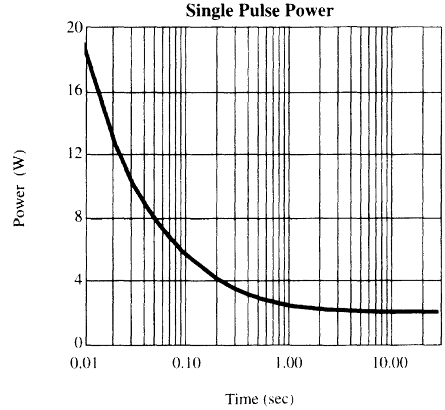
On-Resistance vs. Gate-to-Source Voltage



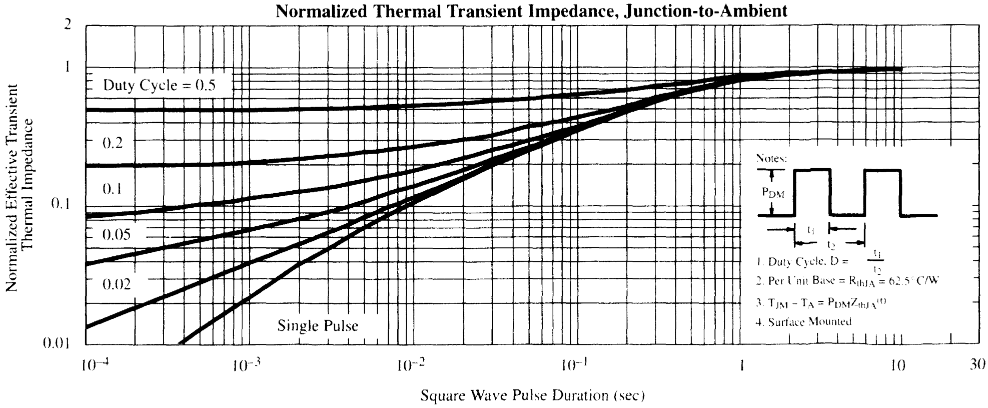
Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient



New Product

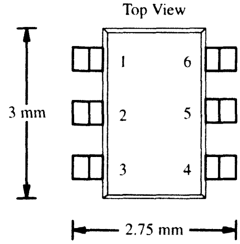
N-Channel Enhancement-Mode MOSFET

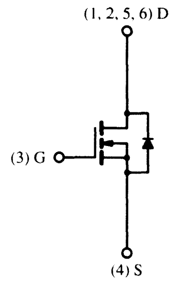
Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
20	0.07 @ V_{GS} = 4.5 V	±4.0
	0.095 @ V_{GS} = 2.5 V	±3.4

2.5-V Rated

TSOP-6
Top View





N-Channel MOSFET

Power Dissipation

Si3442DV—2.0 W

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	±20	V
Gate-Source Voltage		V_{GS}	±8	
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	±4.0	A
	T_A = 70°C		±3.1	
Pulsed Drain Current		I_{DM}	±20	
Continuous Source Current (Diode Conduction)[a]		I_S	±1.6	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	2.0	W
	T_A = 70°C		1.28	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient[a]	R_{thJA}	62.5	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 5 sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70192.

New Product

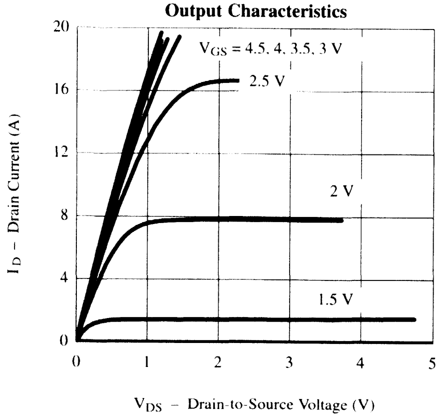
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 µA	0.6			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±8 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V			1	µA
		V_{DS} = 20 V, V_{GS} = 0 V, T_J = 70°C			5	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 4.5 V	10			A
On-State Drain Current[a]		V_{DS} = 5 V, V_{GS} = 2.5 V	4			
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = 4.5 V, I_D = 4.0 A		0.058	0.07	Ω
		V_{GS} = 2.5 V, I_D = 3.4 A		0.072	0.095	
Forward Transconductance[a]	g_{fs}	V_{DS} = 10 V, I_D = 4.0 A		11.3		S
Diode Forward Voltage[a]	V_{SD}	I_S = 1.6 A, V_{GS} = 0 V		0.75	1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = 10 V, V_{GS} = 4.5 V, I_D = 4.0 A		7.0	10	nC
Gate-Source Charge	Q_{gs}			1.1		
Gate-Drain Charge	Q_{gd}			2.0		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 10 V, R_L = 10 Ω I_D ≅ 1 A, V_{GEN} = 4.5 V, R_G = 6 Ω		8	20	ns
Rise Time	t_r			24	40	
Turn-Off Delay Time	$t_{d(off)}$			35	60	
Fall Time	t_f			10	20	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 1.6 A, di/dt = 100 A/µs		40	70	

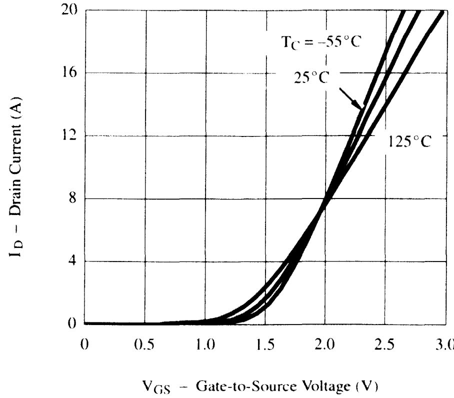
Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

Typical Characteristics (25 °C Unless Otherwise Noted)

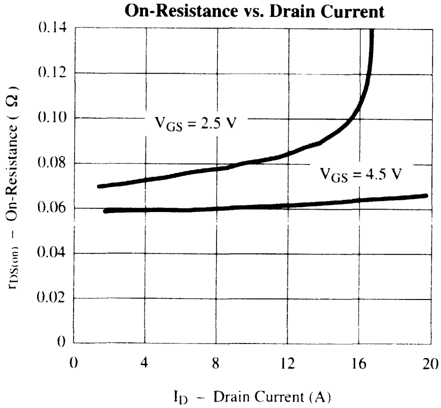
Output Characteristics



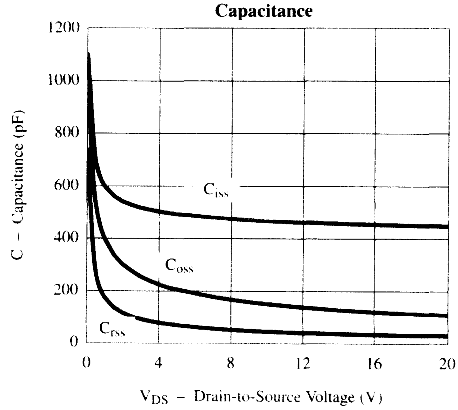
Transfer Characteristics



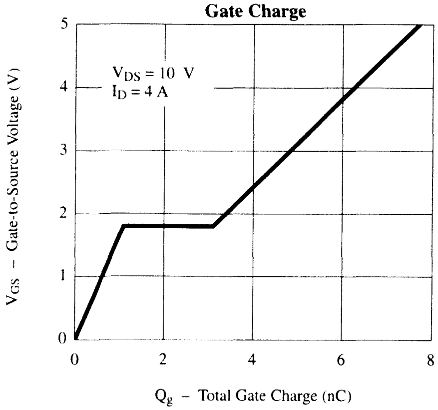
On-Resistance vs. Drain Current



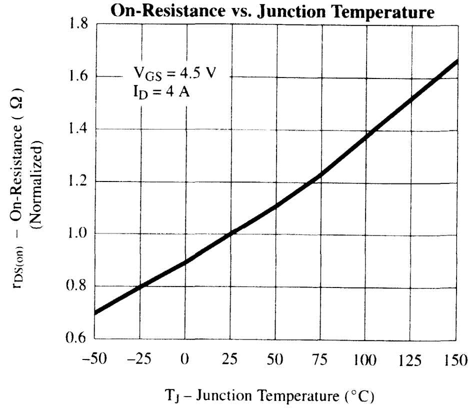
Capacitance



Gate Charge

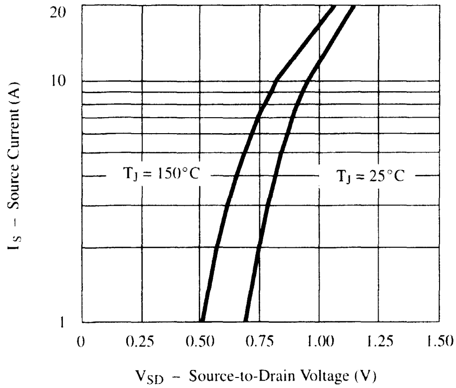


On-Resistance vs. Junction Temperature

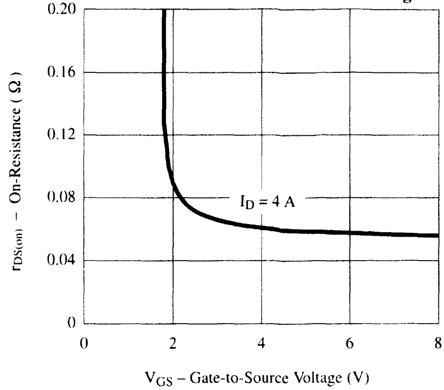


Typical Characteristics (25 °C Unless Otherwise Noted)

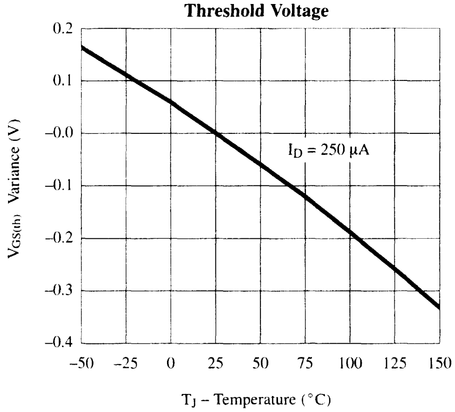
Source-Drain Diode Forward Voltage



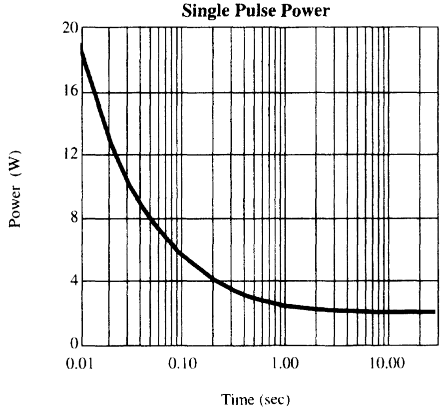
On-Resistance vs. Gate-to-Source Voltage



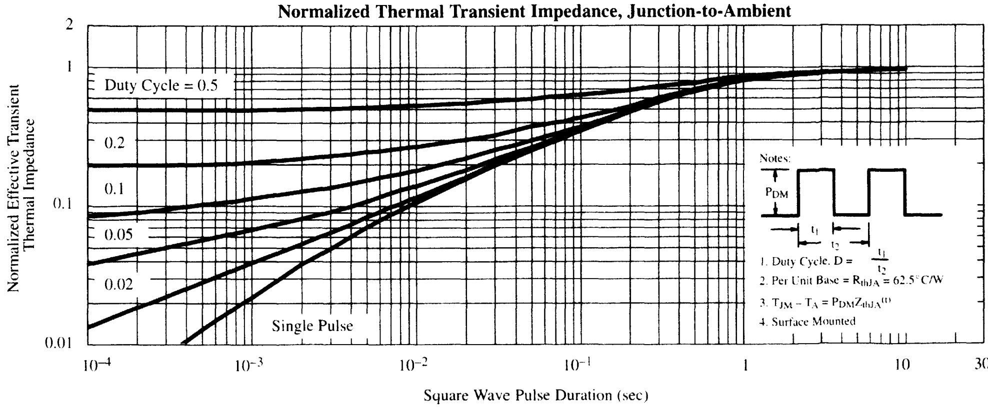
Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient



TEMIC

Semiconductors

Si3454DV

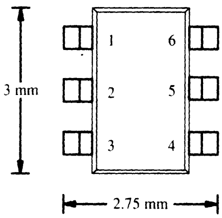
N-Channel Enhancement-Mode MOSFET

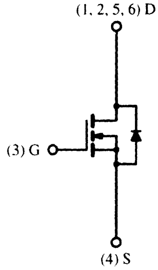
Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
30	0.065 @ V_{GS} = 10 V	± 4.2
	0.095 @ V_{GS} = 4.5 V	± 3.4

TrenchFET™ Power MOSFETS

TSOP-6
Top View





N-Channel MOSFET

Power Dissipation

Si3454DV—2.0 W

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	± 30	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	± 4.2	A
	T_A = 70°C		± 3.4	A
Pulsed Drain Current		I_{DM}	± 20	A
Continuous Source Current (Diode Conduction)[a]		I_S	± 1.7	A
Maximum Power Dissipation[a]	T_A = 25°C	P_D	2.0	W
	T_A = 70°C		1.3	W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient[a]	R_{thJA}	62.5	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 5 sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70193.
A SPICE Model data sheet is available for this product (FaxBack document #70637).

New Product

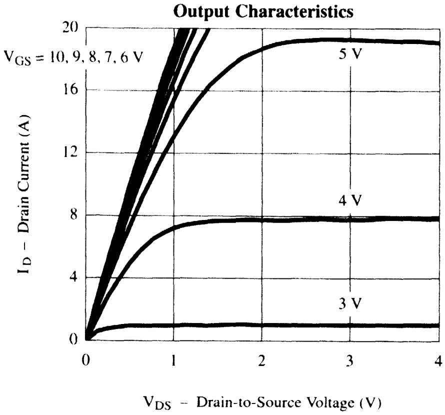
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\ \mu A$	1.0			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = \pm 20$ V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30$ V, $V_{GS} = 0$ V			1	µA
		$V_{DS} = 30$ V, $V_{GS} = 0$ V, $T_J = 70°C$			25	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} = 5$ V, $V_{GS} = 10$ V	15			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	$V_{GS} = 10$ V, $I_D = 4.2$ A		0.050	0.065	Ω
		$V_{GS} = 4.5$ V, $I_D = 3.4$ A		0.070	0.095	
Forward Transconductance[a]	g_{fs}	$V_{DS} = 10$ V, $I_D = 4.2$ A		7		S
Diode Forward Voltage[a]	V_{SD}	$I_S = 1.7$ A, $V_{GS} = 0$ V			1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	$V_{DS} = 10$ V, $V_{GS} = 10$ V, $I_D = 4.2$ A		8	15	nC
Gate-Source Charge	Q_{gs}			1.8		
Gate-Drain Charge	Q_{gd}			1.3		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10$ V, $R_L = 10\ \Omega$ $I_D \cong 1$ A, $V_{GEN} = 10$ V, $R_G = 6\ \Omega$		10	20	ns
Rise Time	t_r			15	30	
Turn-Off Delay Time	$t_{d(off)}$			20	35	
Fall Time	t_f			10	20	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 1.7$ A, di/dt = 100 A/µs		50	80	

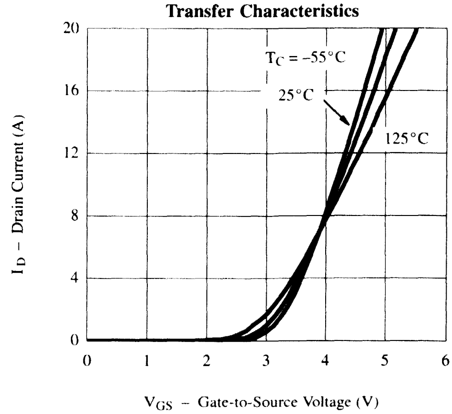
Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

Typical Characteristics (25°C Unless Otherwise Noted)

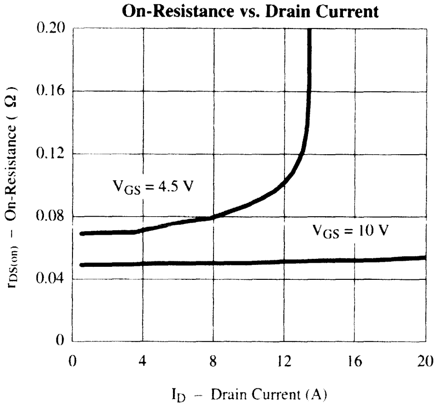
Output Characteristics



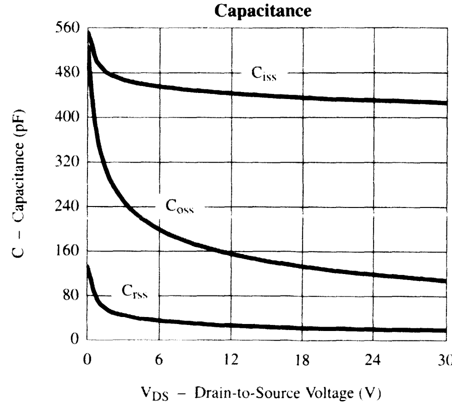
Transfer Characteristics



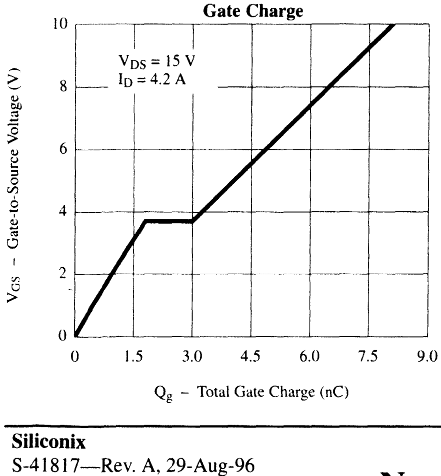
On-Resistance vs. Drain Current



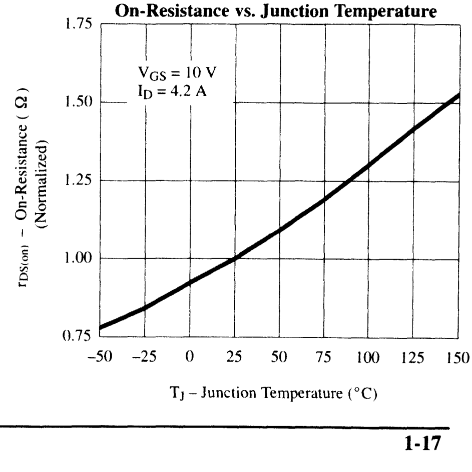
Capacitance



Gate Charge



On-Resistance vs. Junction Temperature



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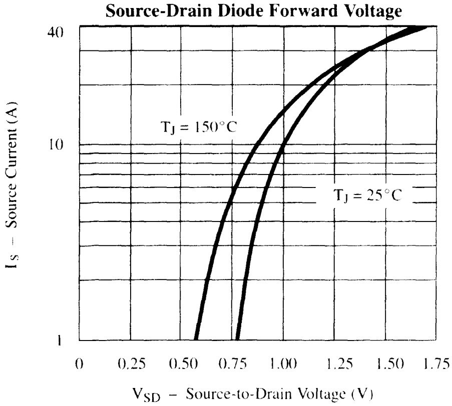
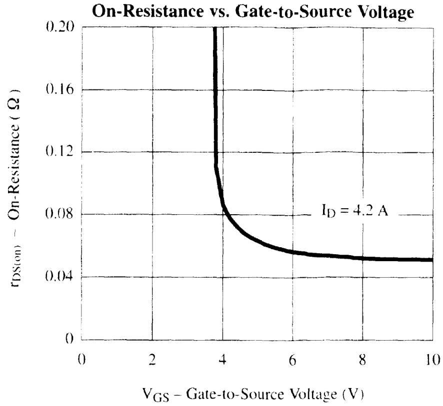
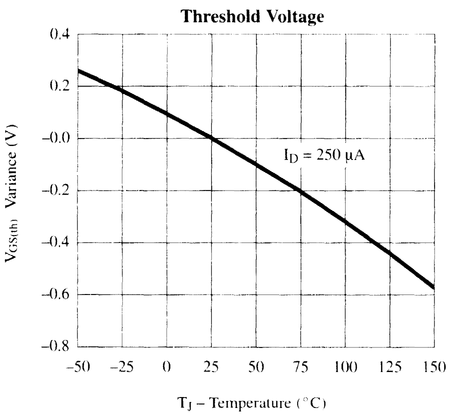
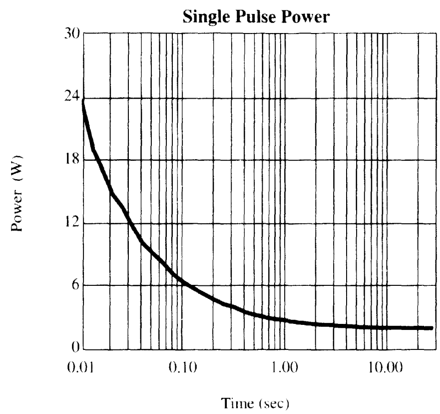
TSOP-6

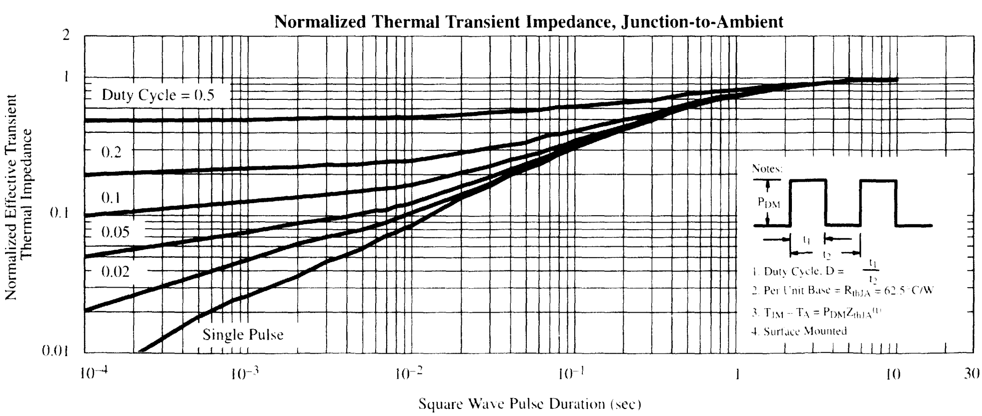
Typical Characteristics (25°C Unless Otherwise Noted)









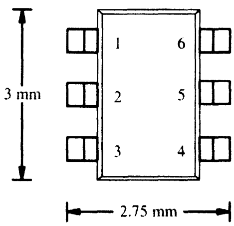


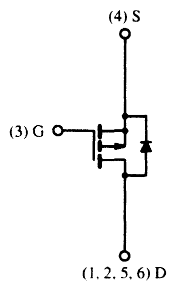
P-Channel Enhancement-Mode MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
–30	0.100 @ V_{GS} = –10 V	±3.5
	0.190 @ V_{GS} = –4.5 V	±2.5

TSOP-6
Top View





P-Channel MOSFET

Power Dissipation

Si3455DV—2.0 W

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	–30	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	±3.5	A
	T_A = 70°C		±2.7	
Pulsed Drain Current		I_{DM}	±20	
Continuous Source Current (Diode Conduction)[a]		I_S	–1.7	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	2.0	W
	T_A = 70°C		1.3	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient[a]	R_{thJA}	62.5	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 5 sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70194.

New Product

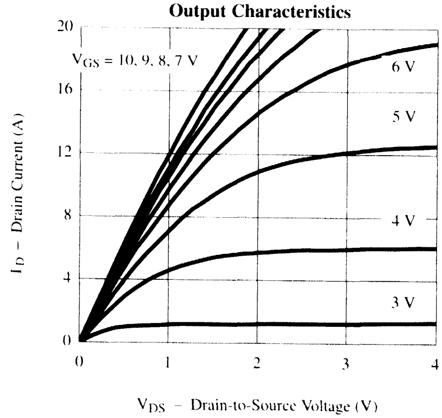
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 µA	−1.0			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = −30 V, V_{GS} = 0 V			−1	µA
		V_{DS} = −30 V, V_{GS} = 0 V, T_J = 70°C			−5	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} = −5 V, V_{GS} = −10 V	−15			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = −10 V, I_D = 3.5 A		0.080	0.100	Ω
		V_{GS} = −4.5 V, I_D = 2.5 A		0.134	0.190	
Forward Transconductance[a]	g_{fs}	V_{DS} = −15 V, I_D = −3.5 A		4.0		S
Diode Forward Voltage[a]	V_{SD}	I_S = −1.7 A, V_{GS} = 0 V			−1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = −10 V, V_{GS} = −10 V, I_D = −3.5 A		5.1	10	nC
Gate-Source Charge	Q_{gs}			1.5		
Gate-Drain Charge	Q_{gd}			1.0		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = −10 V, R_L = 10 Ω I_D ≅ −1 A, V_{GEN} = −10 V, R_G = 6 Ω		10	20	ns
Rise Time	t_r			15	30	
Turn-Off Delay Time	$t_{d(off)}$			20	35	
Fall Time	t_f			10	20	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = −1.7 A, di/dt = 100 A/µs		50	80	

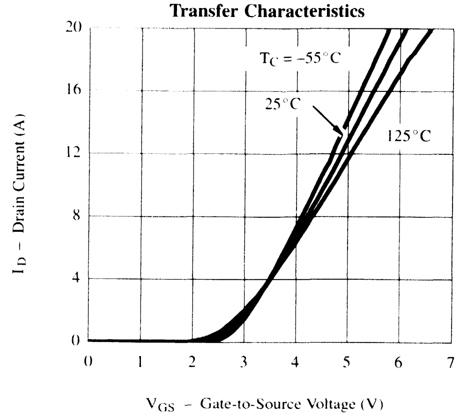
Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

Typical Characteristics (25 °C Unless Otherwise Noted)

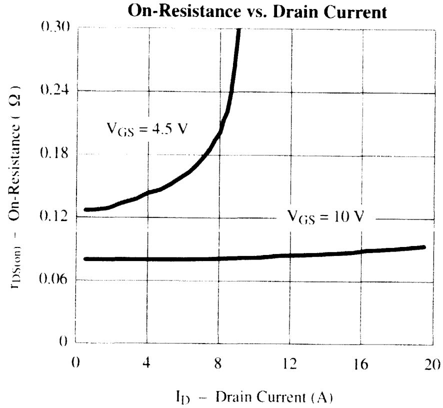
Output Characteristics



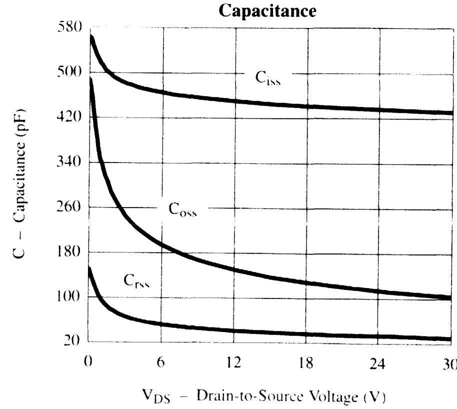
Transfer Characteristics



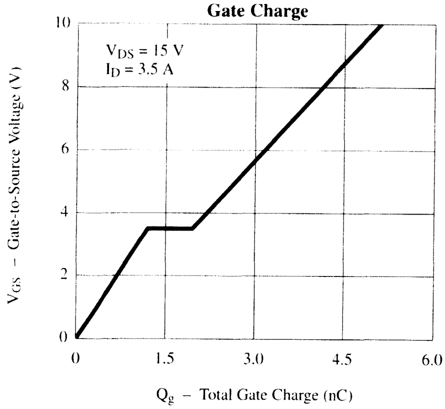
On-Resistance vs. Drain Current



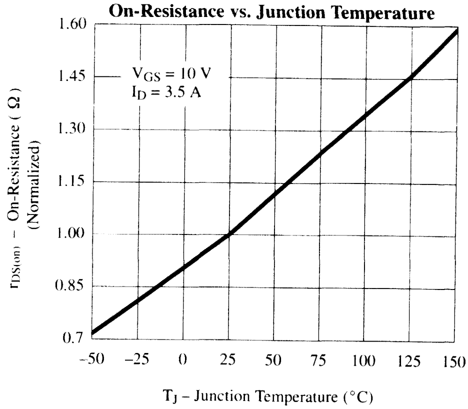
Capacitance



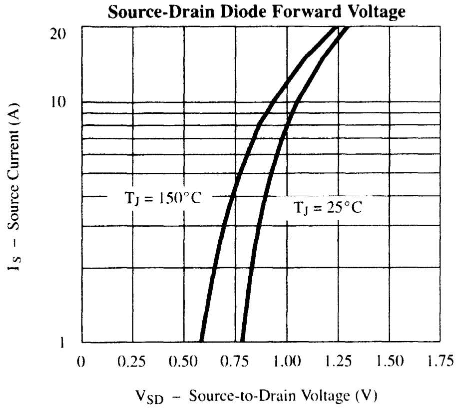
Gate Charge

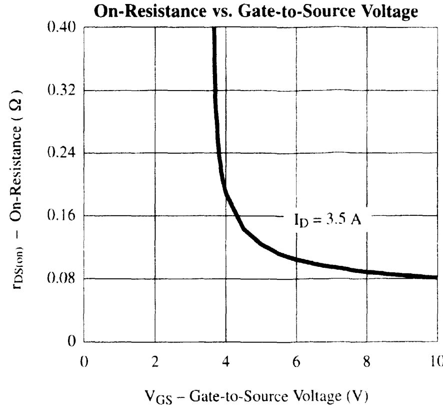


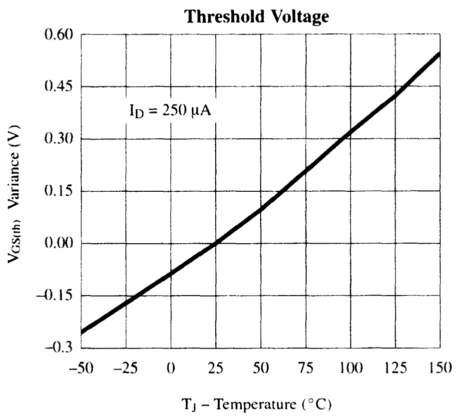
On-Resistance vs. Junction Temperature

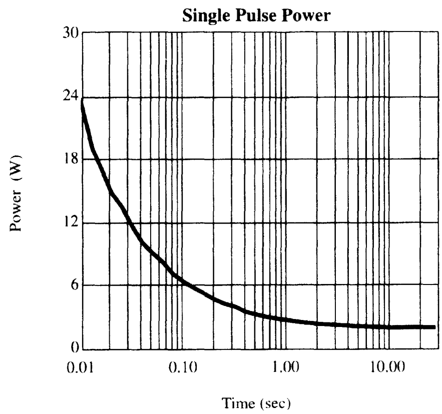


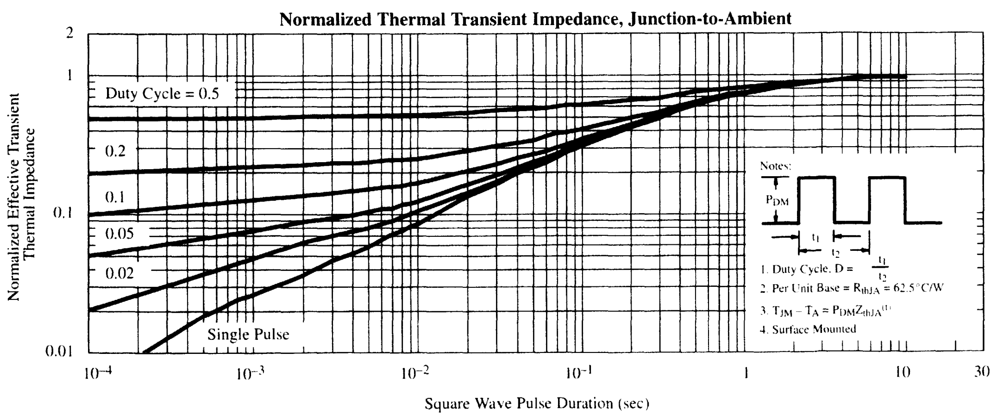
Typical Characteristics (25°C Unless Otherwise Noted)











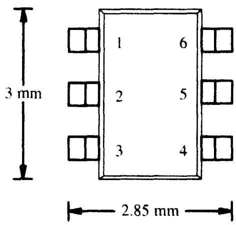
New Product

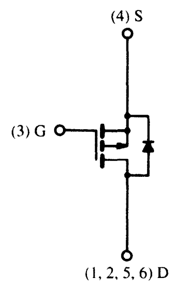
P-Channel 30-V (D-S) Rated MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-30	0.065 @ V_{GS} = –10 V	±4.3
	0.100 @ V_{GS} = –4.5 V	±3.4

TSOP-6
Top View





P-Channel MOSFET

Power Dissipation

Si3457DV—2.0 W

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	±4.3	A
	T_A = 70°C		±3.4	
Pulsed Drain Current		I_{DM}	±20	
Continuous Source Current (Diode Conduction)[a]		I_S	-1.7	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	2	W
	T_A = 70°C		1.3	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient[a]	R_{thJA}	62.5	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 5 sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70644 .

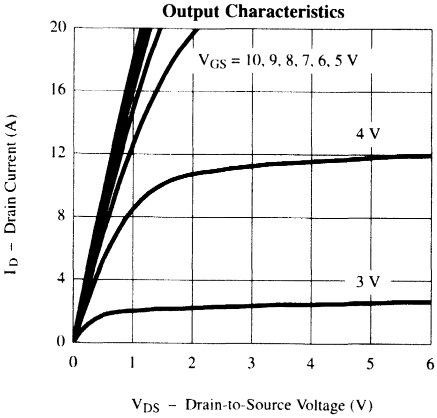
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 µA	−1.0			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = −30 V, V_{GS} = 0 V			−1	µA
		V_{DS} = −30 V, V_{GS} = 0 V, T_J = 70°C			−5	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} = −5 V, V_{GS} = −10 V	−15			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = −10 V, I_D = −4.3 A			0.065	Ω
		V_{GS} = −4.5 V, I_D = −3.4 A			0.100	
Forward Transconductance[a]	g_{fs}	V_{DS} = −15 V, I_D = −4.3 A		6		S
Diode Forward Voltage[a]	V_{SD}	I_S = −1.7 A, V_{GS} = 0 V			−1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = −15 V, V_{GS} = −10 V, I_D = −4.3 A		11	20	nC
Gate-Source Charge	Q_{gs}			2.2		
Gate-Drain Charge	Q_{gd}			1.7		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = −15 V, R_L = 15 Ω I_D ≅ −1 A, V_{GEN} = −10 V, R_G = 6 Ω		7	15	ns
Rise Time	t_r			11	20	
Turn-Off Delay Time	$t_{d(off)}$			30	50	
Fall Time	t_f			11	20	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = −1.7 A, di/dt = 100 A/µs		50	80	

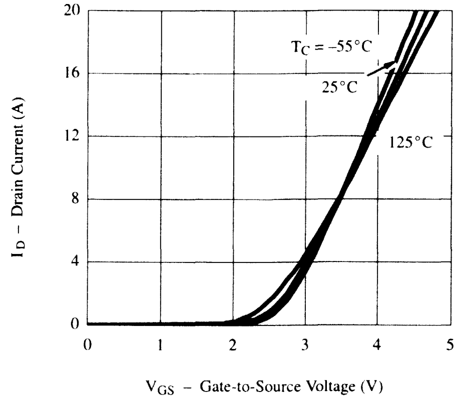
Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

Typical Characteristics (25°C Unless Otherwise Noted)

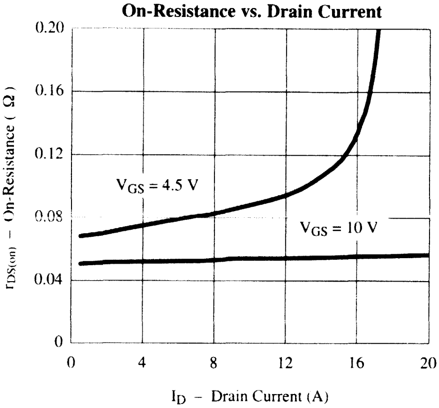
Output Characteristics



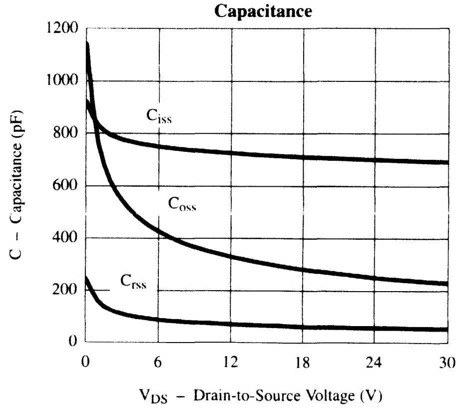
Transfer Characteristics



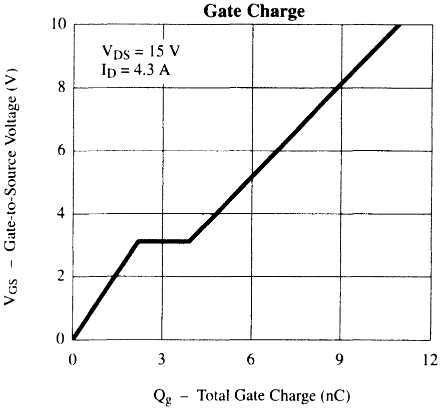
On-Resistance vs. Drain Current



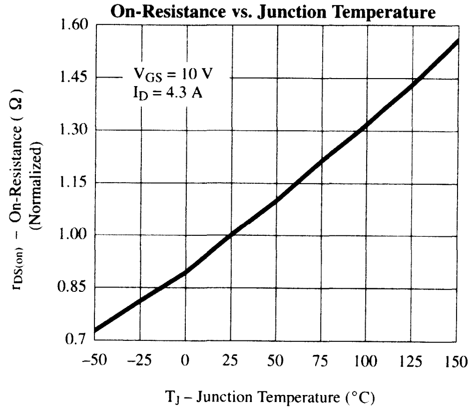
Capacitance



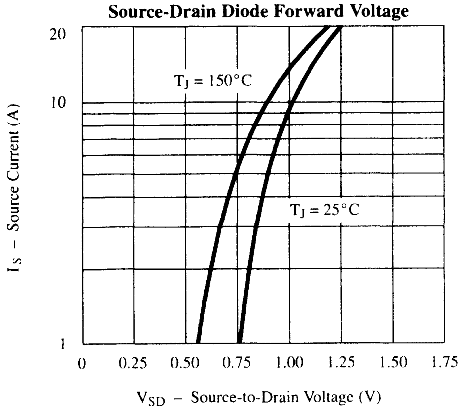
Gate Charge

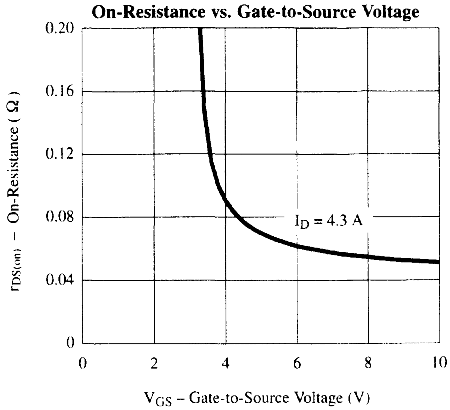


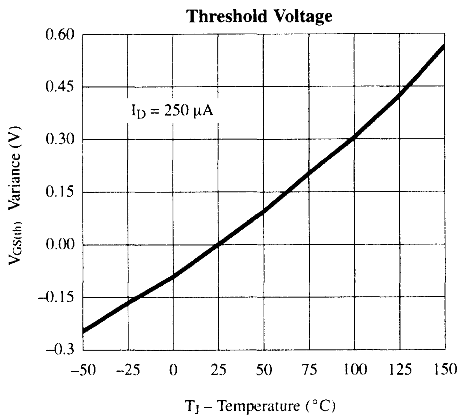
On-Resistance vs. Junction Temperature

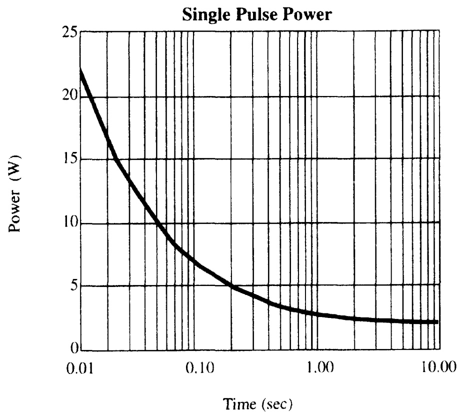


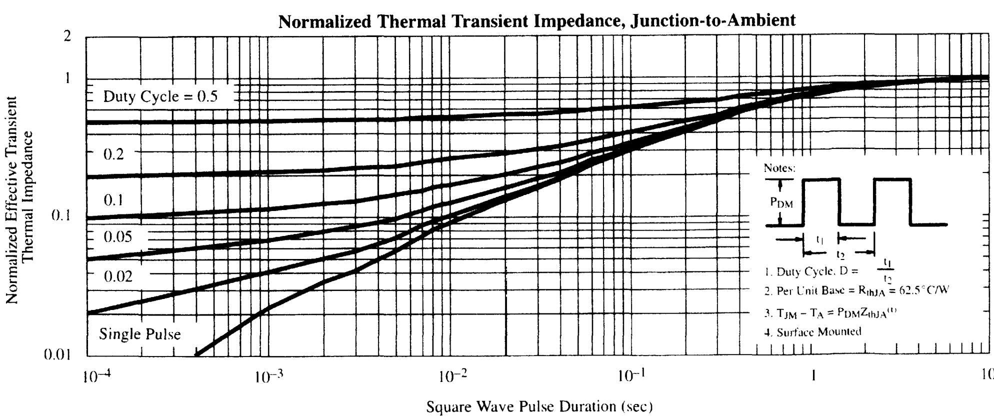
Typical Characteristics (25 °C Unless Otherwise Noted)











New Product

TEMIC
Semiconductors

Si6415DQ

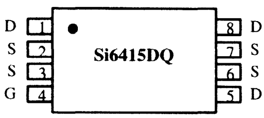
P-Channel 30-V (D-S) Rated MOSFET

Product Summary

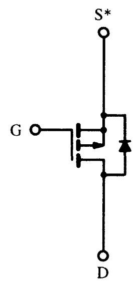
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
–30	0.019 @ V_{GS} = –10 V	± 6.5
	0.030 @ V_{GS} = –4.5 V	± 5.2

TrenchFET™ Power MOSFETS

TSSOP-8



Top View



*Source Pins 2, 3, 6 and 7 must be tied common.

P-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	–30	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	± 6.5	A
	T_A = 70°C		± 5.2	
Pulsed Drain Current		I_{DM}	± 30	
Continuous Source Current (Diode Conduction)[a]		I_S	–1.5	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	1.5	W
	T_A = 70°C		1.0	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient[a]	R_{thJA}	83	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70639.

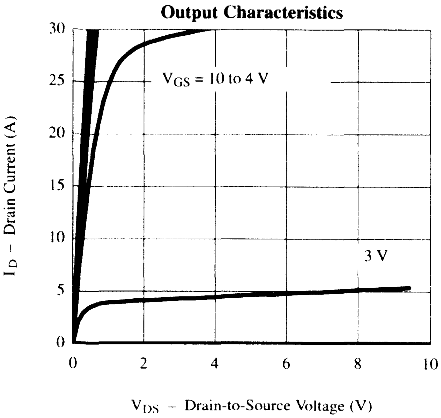
New Product

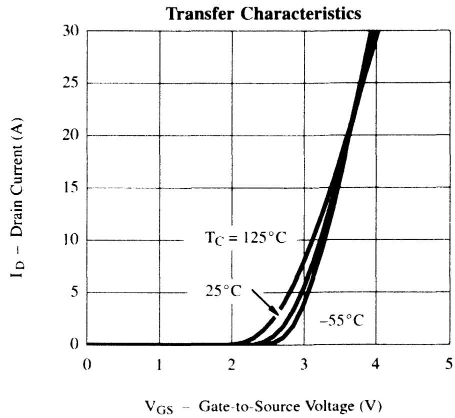
Specifications (T_J = 25°C Unless Otherwise Noted)

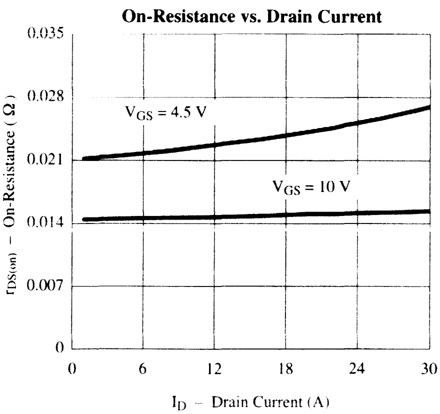
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250\ \mu A$	−1.0			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = \pm 20$ V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -30$ V, $V_{GS} = 0$ V			−1	µA
		$V_{DS} = -30$ V, $V_{GS} = 0$ V, $T_J = 55°C$			−25	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} = -5$ V, $V_{GS} = -10$ V	−20			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	$V_{GS} = -10$ V, $I_D = -6.5$ A		0.015	0.019	Ω
		$V_{GS} = -4.5$ V, $I_D = -5.2$ A		0.022	0.030	
Forward Transconductance[a]	g_{fs}	$V_{DS} = -15$ V, $I_D = -6.5$ A		18.5		S
Diode Forward Voltage[a]	V_{SD}	$I_S = -1.5$ A, $V_{GS} = 0$ V		−0.75	−1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	$V_{DS} = -15$ V, $V_{GS} = -10$ V, $I_D = -6.5$ A		47	70	nC
Gate-Source Charge	Q_{gs}			9.5		
Gate-Drain Charge	Q_{gd}			8		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -15$ V, $R_L = 15\ \Omega$ $I_D \cong -1$ A, $V_{GEN} = -10$ V, $R_G = 6\ \Omega$		16	30	ns
Rise Time	t_r			17	30	
Turn-Off Delay Time	$t_{d(off)}$			73	110	
Fall Time	t_f			31	60	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -1.5$ A, di/dt = 100 A/µs		40	60	

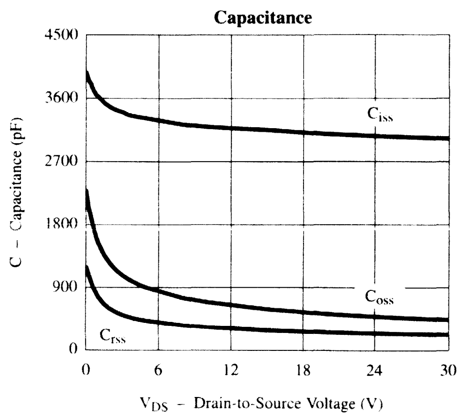
Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

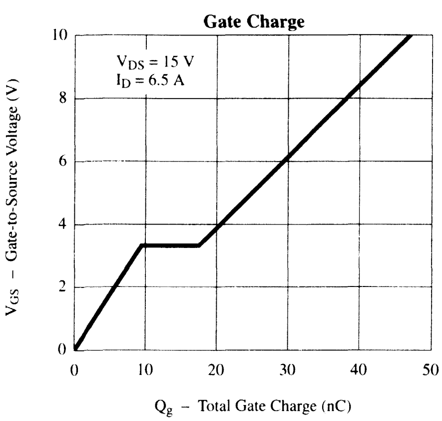
Typical Characteristics (25°C Unless Noted)

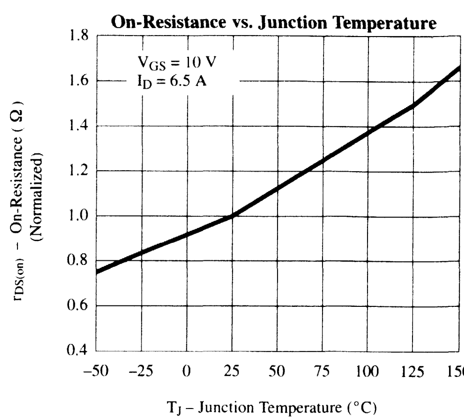




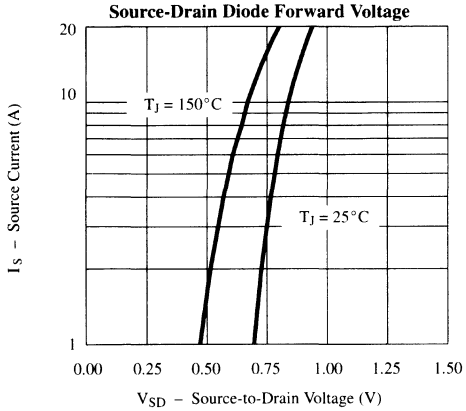


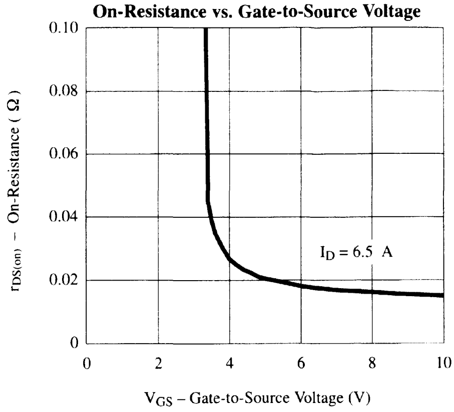


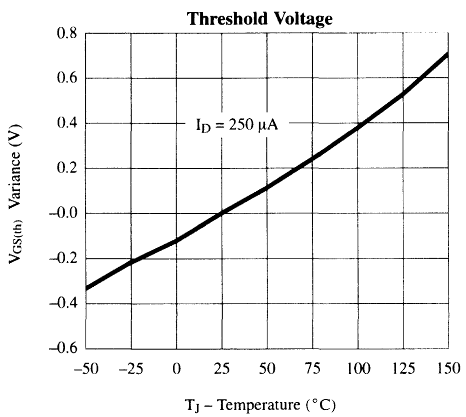


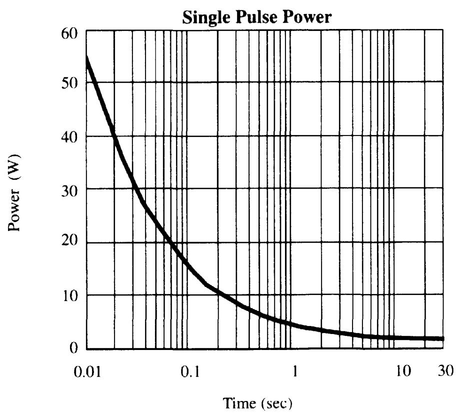


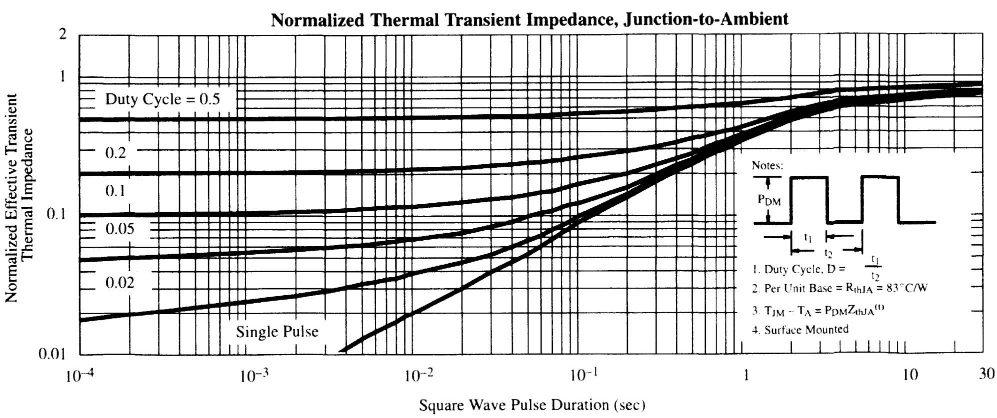
Typical Characteristics (25°C Unless Noted)











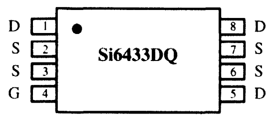
New Product

P-Channel Enhancement-Mode MOSFET

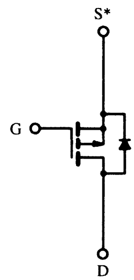
Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
–12	0.06 @ V_{GS} = –4.5 V	±4.0
	0.09 @ V_{GS} = –2.5 V	±3.0

TSSOP-8



Top View



*Source Pins 2, 3, 6 and 7 must be tied common.

P-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	–12	V
Gate-Source Voltage		V_{GS}	±8	
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	±4.0	A
	T_A = 70°C		±3.2	
Pulsed Drain Current		I_{DM}	±20	
Continuous Source Current (Diode Conduction)[a]		I_S	–1.4	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	1.5	W
	T_A = 70°C		1.0	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient[a]	R_{thJA}	83	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 10 sec.

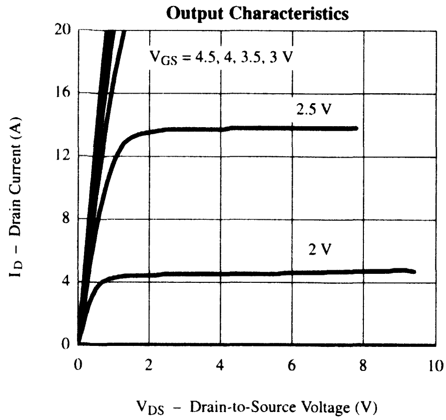
Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70168. A SPICE Model data sheet is available for this product (FaxBack document #70530).

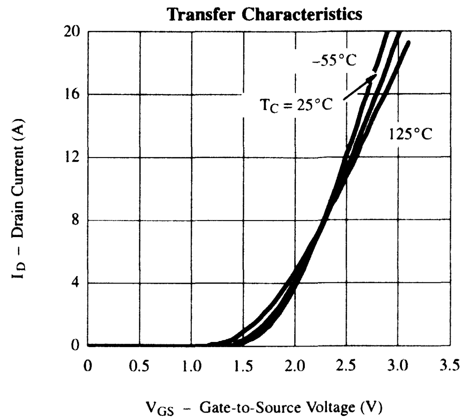
Specifications (T_J = 25°C Unless Otherwise Noted)

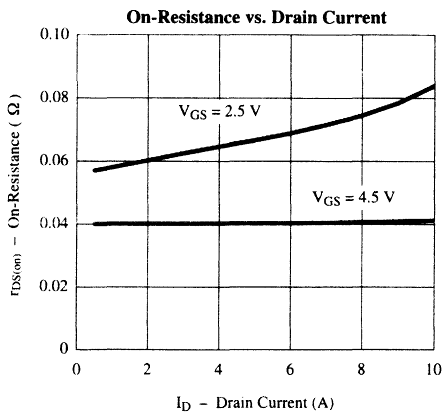
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 µA	–0.6			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±8 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = –12 V, V_{GS} = 0 V			–1	µA
		V_{DS} = –12 V, V_{GS} = 0 V, T_J = 70°C			–25	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} = –5 V, V_{GS} = –4.5 V	–10			A
		V_{DS} = –5 V, V_{GS} = –2.5 V	–4			
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = –4.5 V, I_D = 4.0 A		0.040	0.06	Ω
		V_{GS} = –2.5 V, I_D = 2.0 A		0.060	0.09	
Forward Transconductance[a]	g_{fs}	V_{DS} = –9 V, I_D = –4.0 A		13		S
Diode Forward Voltage[a]	V_{SD}	I_S = –1.4 A, V_{GS} = 0 V		–0.8	–1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = –6 V, V_{GS} = –4.5 V, I_D = –4.0 A		20	40	nC
Gate-Source Charge	Q_{gs}			3.5		
Gate-Drain Charge	Q_{gd}			6.0		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = –6 V, R_L = 6 Ω I_D ≅ –1 A, V_{GEN} = –4.5 V, R_G = 6 Ω		26	60	ns
Rise Time	t_r			47	100	
Turn-Off Delay Time	$t_{d(off)}$			87	180	
Fall Time	t_f			47	100	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = –1.4 A, di/dt = 100 A/µs		70	100	

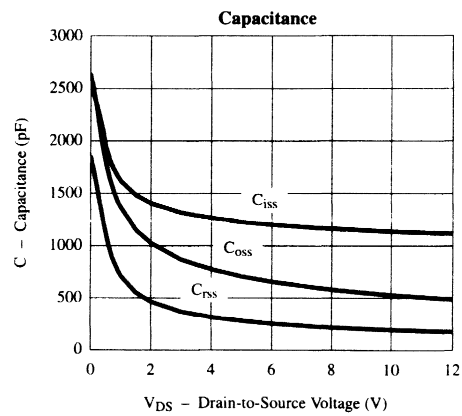
Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

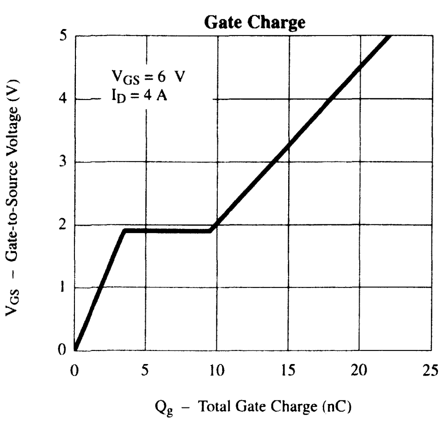
Typical Characteristics (25 °C Unless Otherwise Noted)

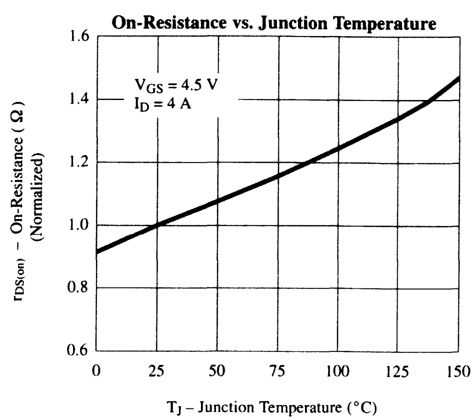






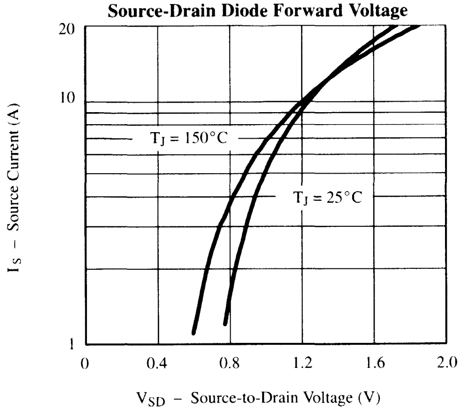




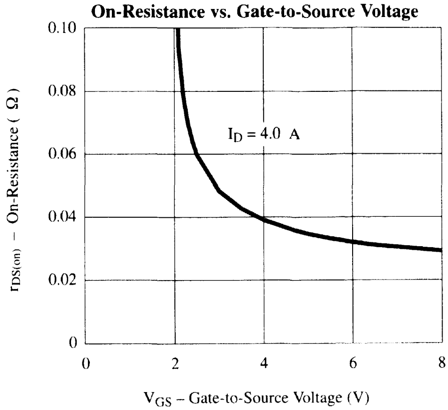


Typical Characteristics (25° C Unless Noted)

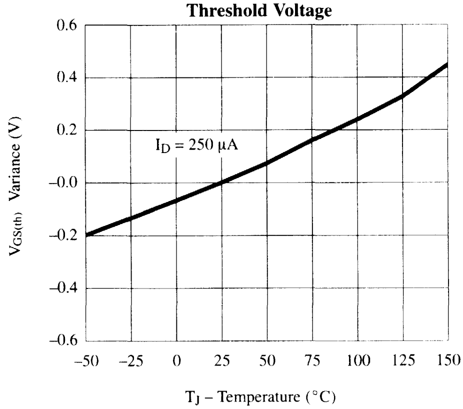
Source-Drain Diode Forward Voltage



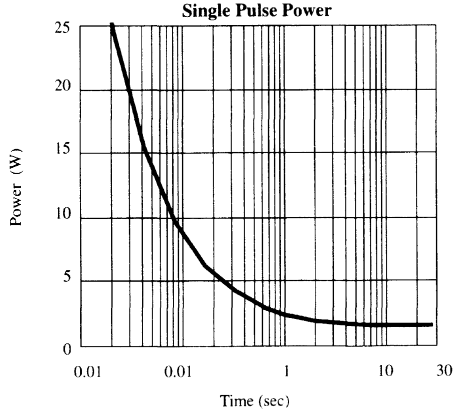
On-Resistance vs. Gate-to-Source Voltage



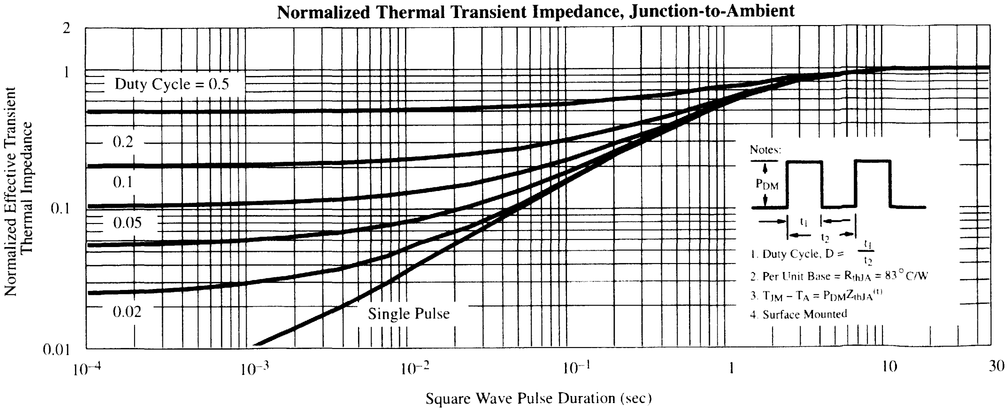
Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient



N-Channel Enhancement-Mode MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
30	0.028 @ V_{GS} = 10 V	±5.6
	0.042 @ V_{GS} = 4.5 V	±4.5

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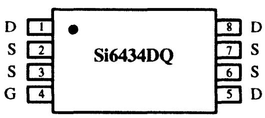
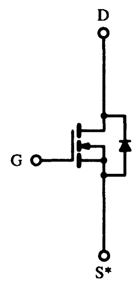


Top View



*Source Pins 2, 3, 6 and 7 must be tied common.

N-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	±5.6	A
	T_A = 70°C		±4.4	
Pulsed Drain Current		I_{DM}	±30	
Continuous Source Current (Diode Conduction)[a]		I_S	1.25	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	1.5	W
	T_A = 70°C		1.0	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient[a]	R_{thJA}	83	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 10 sec.

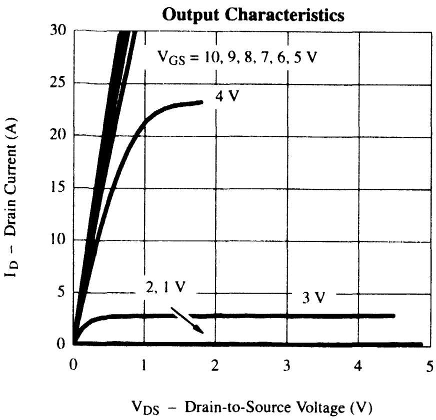
Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70178. A SPICE Model data sheet is available for this product (FaxBack document #70562).

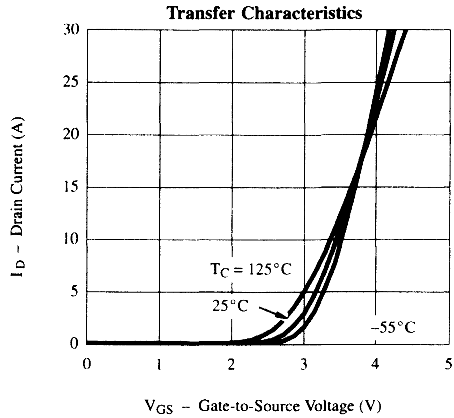
Specifications (T_J = 25°C Unless Otherwise Noted)

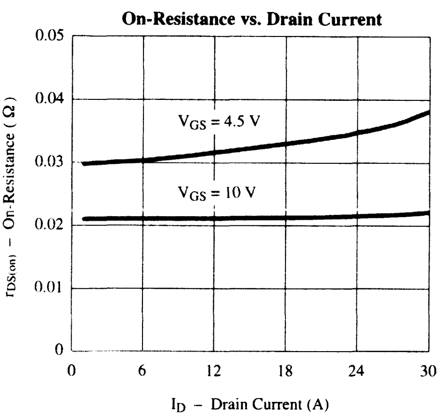
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 μA	1			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V			1	μA
		V_{DS} = 30 V, V_{GS} = 0 V, T_J = 55°C			25	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 10 V	20			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 5.6 A		0.022	0.028	Ω
		V_{GS} = 4.5 V, I_D = 3.5 A		0.030	0.042	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 5.6 A		14		S
Diode Forward Voltage[a]	V_{SD}	I_S = 1.25 A, V_{GS} = 0 V		0.75	1.1	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = 15 V, V_{GS} = 10 V, I_D = 5.6 A		18	29	nC
Gate-Source Charge	Q_{gs}			3.3		
Gate-Drain Charge	Q_{gd}			2.6		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 15 V, R_L = 15 Ω I_D ≅ 1 A, V_{GEN} = 10 V, R_G = 6 Ω		9	15	ns
Rise Time	t_r			12	20	
Turn-Off Delay Time	$t_{d(off)}$			38	55	
Fall Time	t_f			19	28	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 1.25 A, di/dt = 100 A/μs		45		

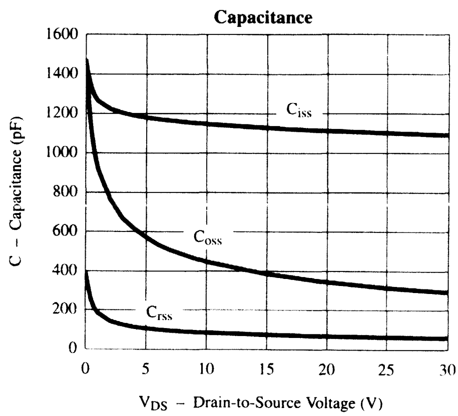
Notes
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

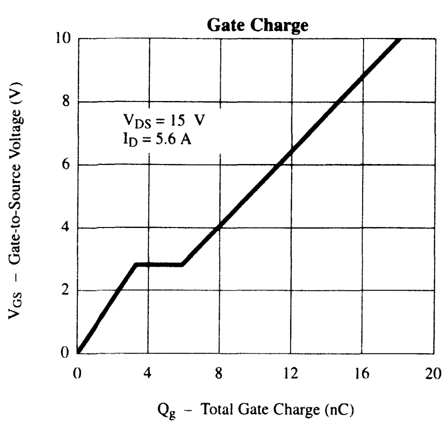
Typical Characteristics (25°C Unless Noted)

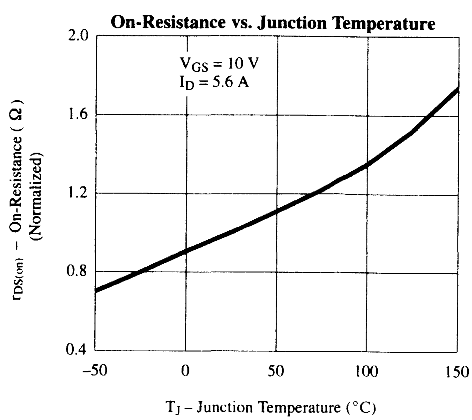












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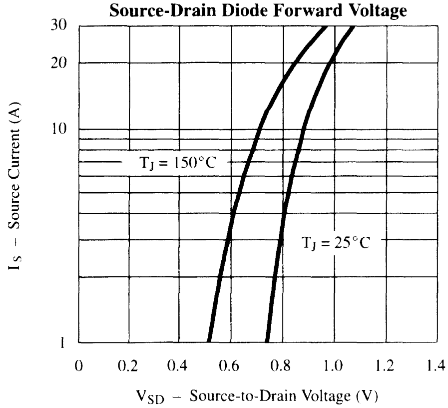
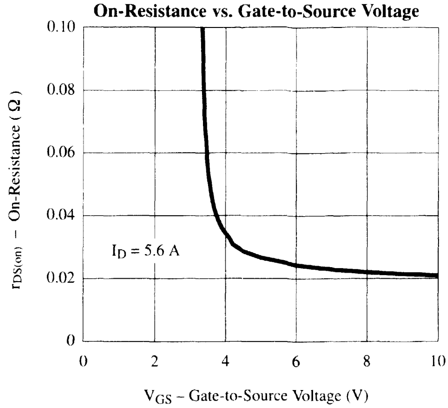
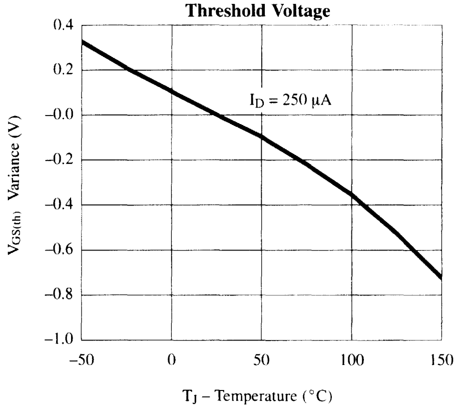
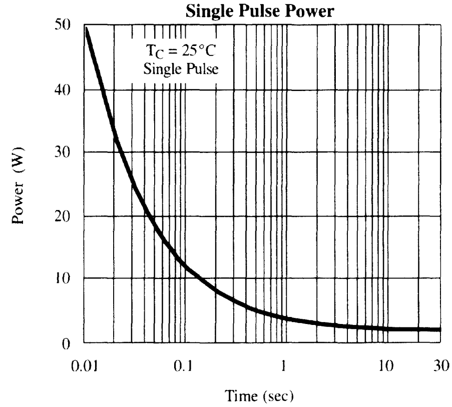
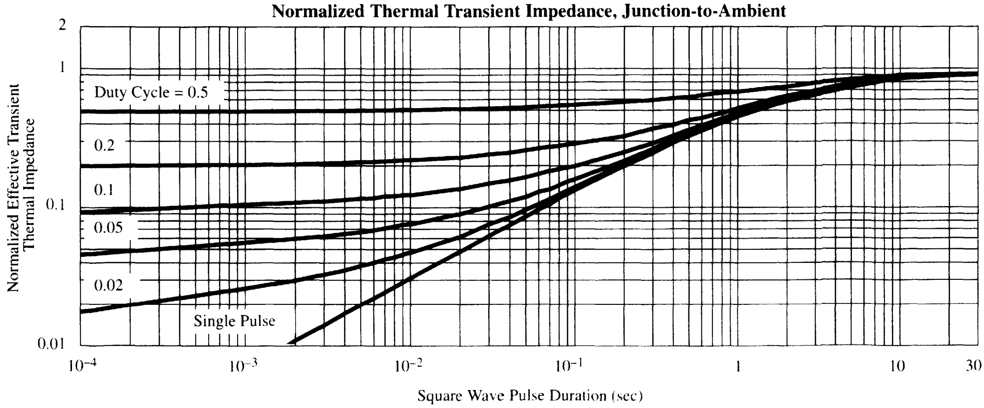
Typical Characteristics (25°C Unless Otherwise Noted)











P-Channel Enhancement-Mode MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
–30	0.040 @ V_{GS} = –10 V	±4.5
	0.070 @ V_{GS} = –4.5 V	±3.4

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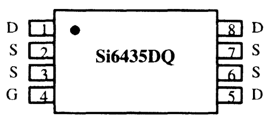
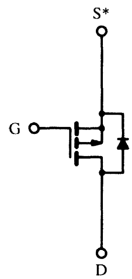


Top View



*Source Pins 2, 3, 6 and 7 must be tied common.

P-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	–30	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	±4.5	A
	T_A = 70°C		±3.6	
Pulsed Drain Current		I_{DM}	±30	
Continuous Source Current (Diode Conduction)[a]		I_S	–1.25	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	1.5	W
	T_A = 70°C		1.0	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient[a]	R_{thJA}	83	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70182. A SPICE Model data sheet is available for this product (FaxBack document #70546).

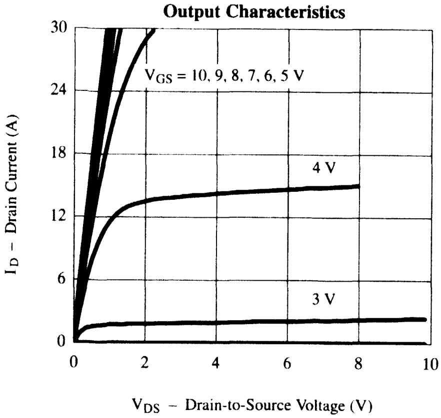
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250\ \mu A$	−1.0			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = \pm 20$ V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -30$ V, $V_{GS} = 0$ V			−1	µA
		$V_{DS} = -30$ V, $V_{GS} = 0$ V, $T_J = 70°C$			−25	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} = -5$ V, $V_{GS} = -10$ V	−30			A
		$V_{DS} = -5$ V, $V_{GS} = -4.5$ V	−7			
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	$V_{GS} = -10$ V, $I_D = -4.5$ A		0.029	0.040	Ω
		$V_{GS} = -4.5$ V, $I_D = -3.4$ A		0.047	0.070	
Forward Transconductance[a]	g_{fs}	$V_{DS} = -15$ V, $I_D = -4.5$ A		9.3		S
Diode Forward Voltage[a]	V_{SD}	$I_S = -1.25$ A, $V_{GS} = 0$ V		−0.8	−1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	$V_{DS} = -15$ V, $V_{GS} = -10$ V, $I_D = -4.5$ A		25	35	nC
Gate-Source Charge	Q_{gs}			5.0		
Gate-Drain Charge	Q_{gd}			4.0		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -15$ V, $R_L = 15\ \Omega$ $I_D \cong -1$ A, $V_{GEN} = -10$ V, $R_G = 6\ \Omega$		12	20	ns
Rise Time	t_r			13	20	
Turn-Off Delay Time	$t_{d(off)}$			40	55	
Fall Time	t_f			16	25	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -1.25$ A, di/dt = 100 A/µs		50	80	

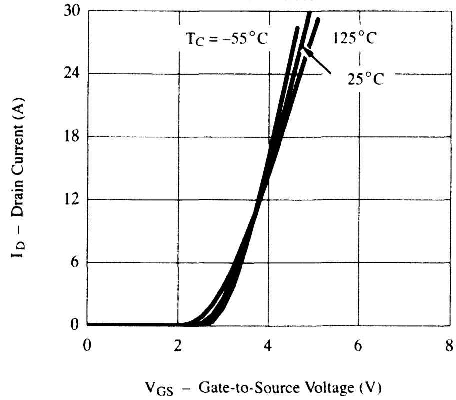
Notes
a. Pulse test: pulse width ≤ 300 µs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

Typical Characteristics (25 °C Unless Noted)

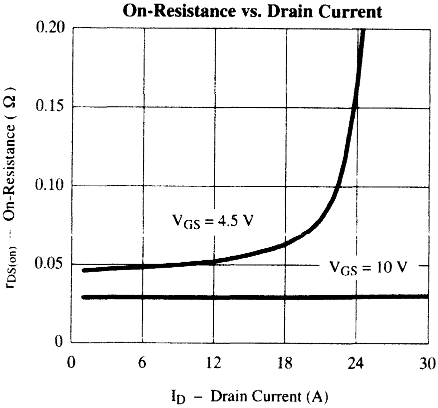
Output Characteristics



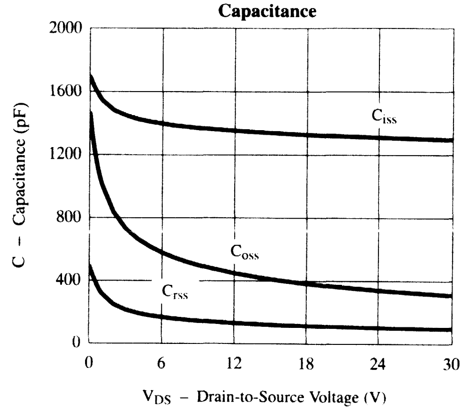
Transfer Characteristics



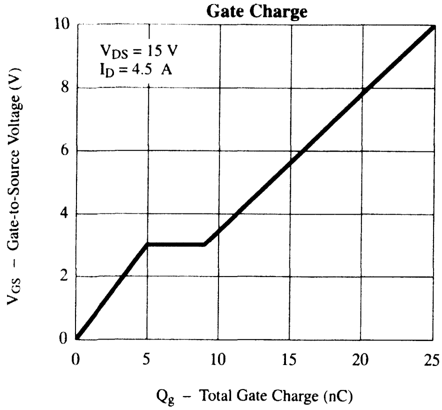
On-Resistance vs. Drain Current



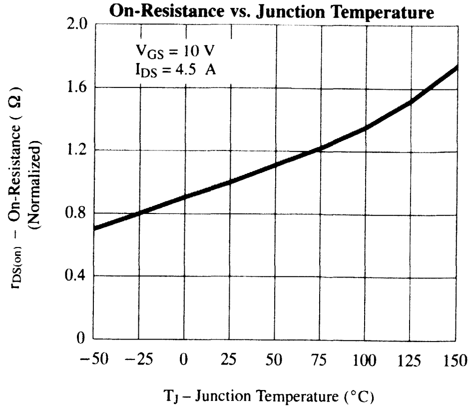
Capacitance



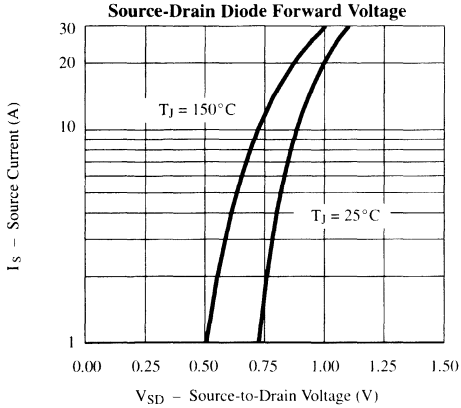
Gate Charge

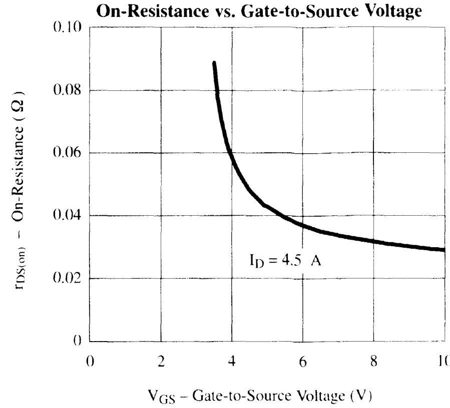


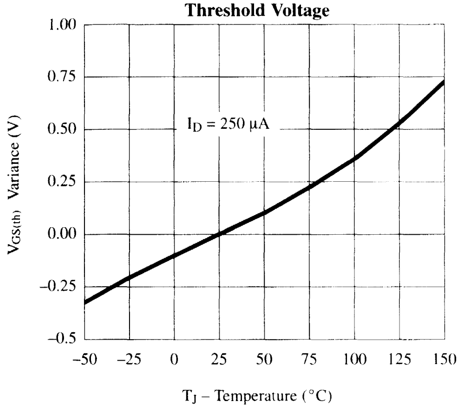
On-Resistance vs. Junction Temperature

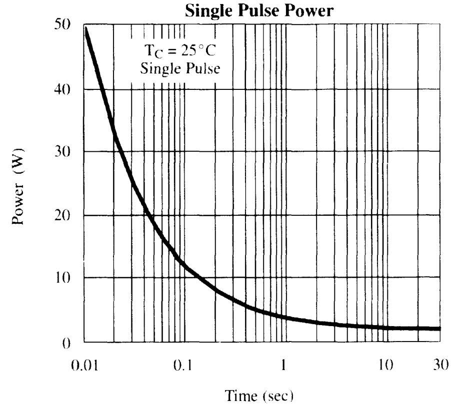


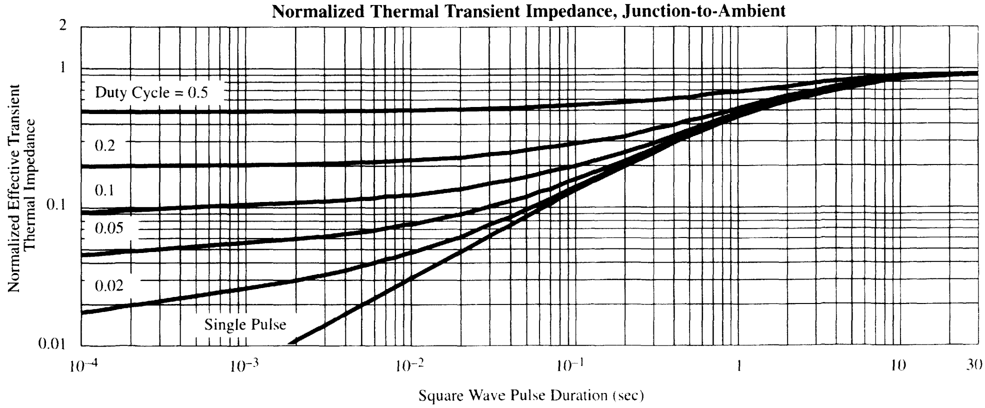
Typical Characteristics (25 °C Unless Noted)











P-Channel 60-V (D-S) Rated MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
–60	0.120 @ V_{GS} = –10 V	±2.6
	0.150 @ V_{GS} = –4.5 V	±2.4

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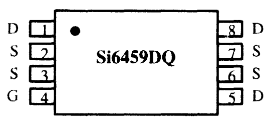
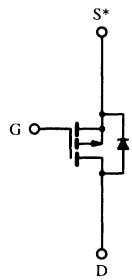


Top View



*Source Pins 2, 3, 6 and 7 must be tied common.

P-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	–60	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	±2.6	A
	T_A = 70°C		±2.1	
Pulsed Drain Current		I_{DM}	±30	
Continuous Source Current (Diode Conduction)[a]		I_S	–1.25	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	1.5	W
	T_A = 70°C		1.0	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient[a]	R_{thJA}	83	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70186.

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TSSOP-8/-28

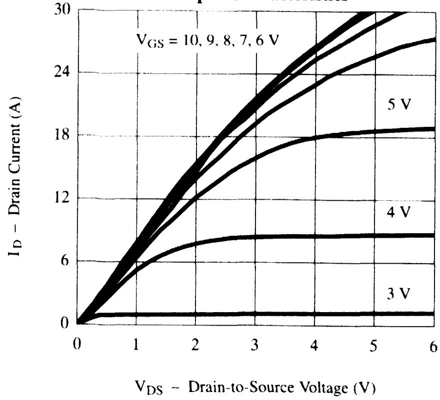
Specifications ($T_J = 25°C$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250\ \mu A$	-1.0			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = \pm 20$ V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -60$ V, $V_{GS} = 0$ V			-1	µA
		$V_{DS} = -60$ V, $V_{GS} = 0$ V, $T_J = 70°C$			-25	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} = -5$ V, $V_{GS} = -10$ V	-20			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	$V_{GS} = -10$ V, $I_D = -2.6$ A		0.100	0.120	Ω
		$V_{GS} = -4.5$ V, $I_D = -2.4$ A		0.125	0.150	
Forward Transconductance[a]	g_{fs}	$V_{DS} = -15$ V, $I_D = -2.6$ A		7.5		S
Diode Forward Voltage[a]	V_{SD}	$I_S = -1.25$ A, $V_{GS} = 0$ V		-0.8	-1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	$V_{DS} = -30$ V, $V_{GS} = -10$ V, $I_D = -2.6$ A		16	25	nC
Gate-Source Charge	Q_{gs}			3.7		
Gate-Drain Charge	Q_{gd}			2.0		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -30$ V, $R_L = 30\ \Omega$, $I_D \cong -1$ A, $V_{GEN} = -10$ V, $R_G = 6\ \Omega$		8	15	ns
Rise Time	t_r			10	20	
Turn-Off Delay Time	$t_{d(off)}$			12	25	
Fall Time	t_f			35	50	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -1.25$ A, di/dt = 100 A/µs		60	90	

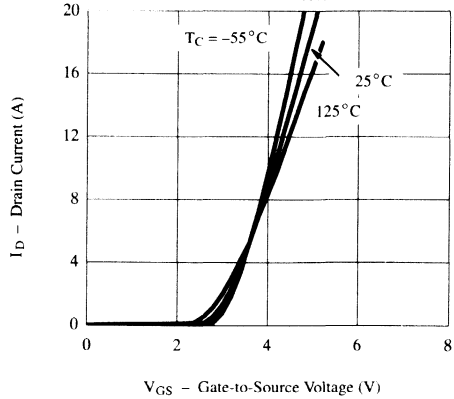
Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

Typical Characteristics (25 °C Unless Noted)

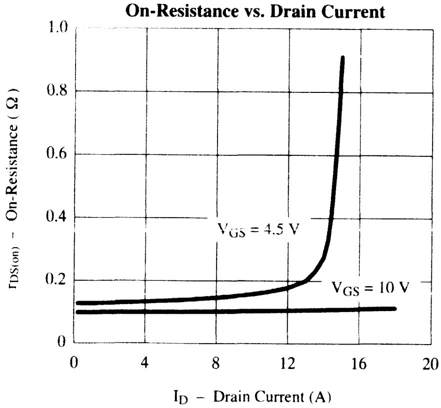
Output Characteristics



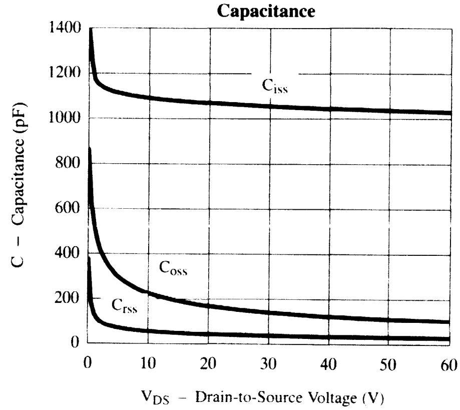
Transfer Characteristics



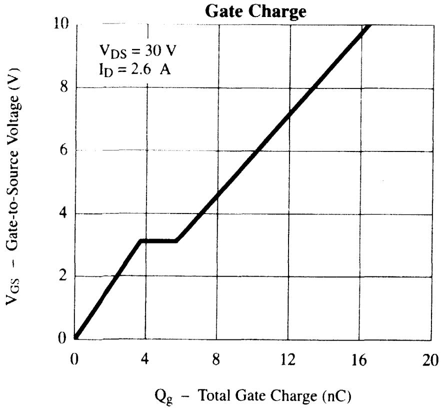
On-Resistance vs. Drain Current



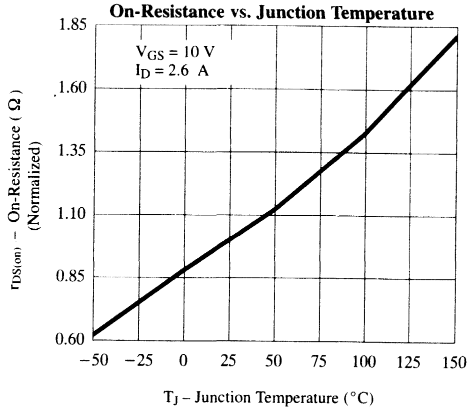
Capacitance



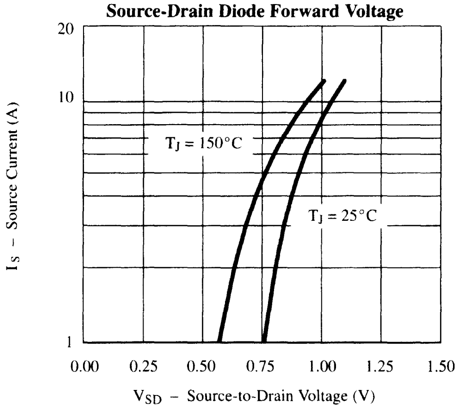
Gate Charge

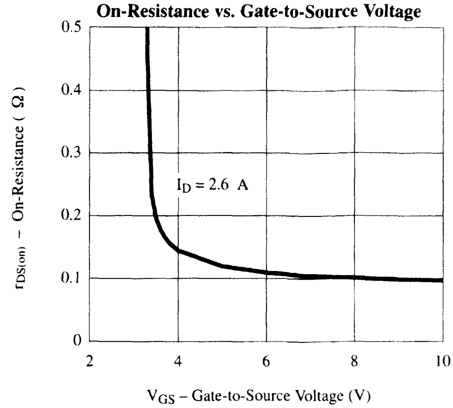


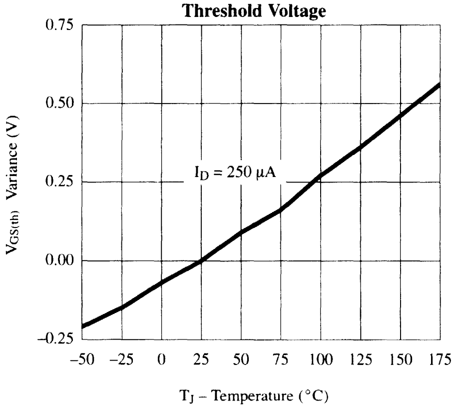
On-Resistance vs. Junction Temperature

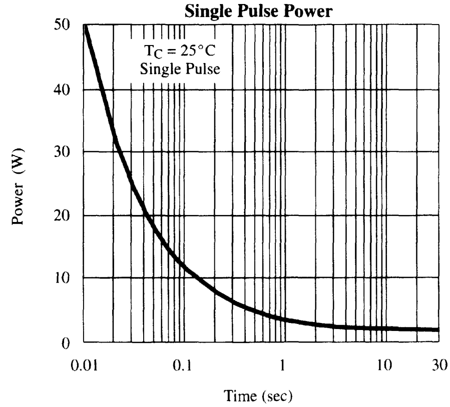


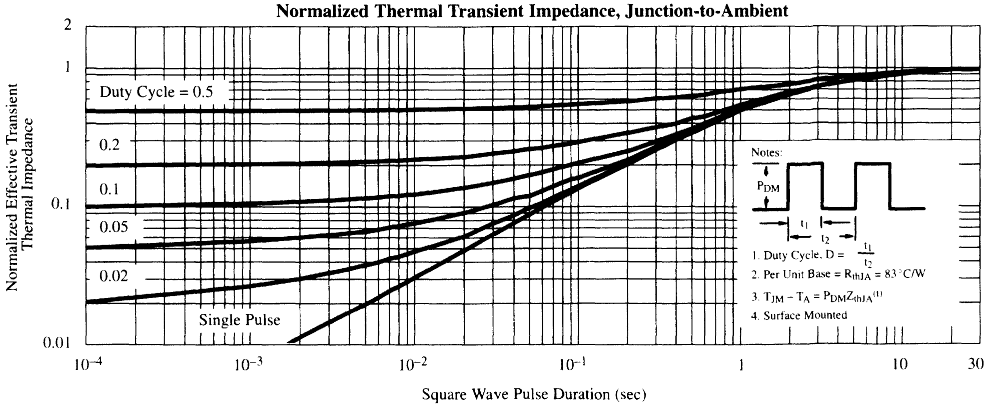
Typical Characteristics (25° C Unless Noted)











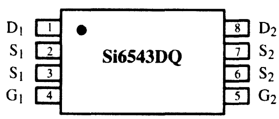
New Product

Dual Enhancement-Mode MOSFET (N- and P-Channel)

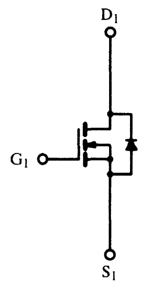
Product Summary

	V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
N-Channel	30	0.065 @ V_{GS} = 10 V	± 3.9
		0.095 @ V_{GS} = 4.5 V	± 3.1
P-Channel	–30	0.085 @ V_{GS} = –10 V	± 2.5
		0.19 @ V_{GS} = –4.5 V	± 1.8

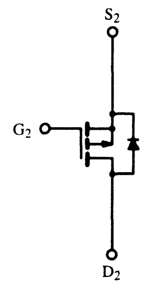
TSSOP-8



Top View



N-Channel MOSFET



P-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage		V_{DS}	30	–30	V
Gate-Source Voltage		V_{GS}	± 20	± 20	V
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	± 3.9	± 2.5	A
	T_A = 70°C		± 3.1	± 2.1	A
Pulsed Drain Current		I_{DM}	± 20	± 20	A
Continuous Source Current (Diode Conduction)[a]		I_S	1.25	–1.25	A
Maximum Power Dissipation[a]	T_A = 25°C	P_D	1.0		W
	T_A = 70°C		0.64		W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150		°C

Thermal Resistance Ratings

Parameter	Symbol	N- or P-Channel	Unit
Maximum Junction-to-Ambient[a]	R_{thJA}	125	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70181. A SPICE Model data sheet is available for this product (FaxBack document #70547).

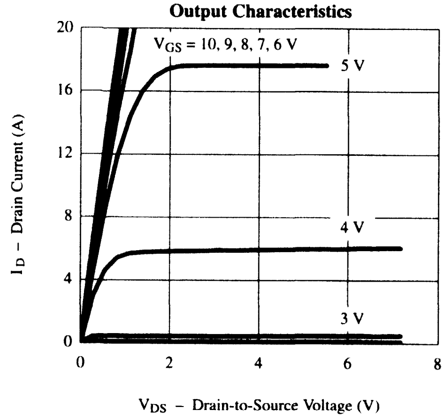
New Product

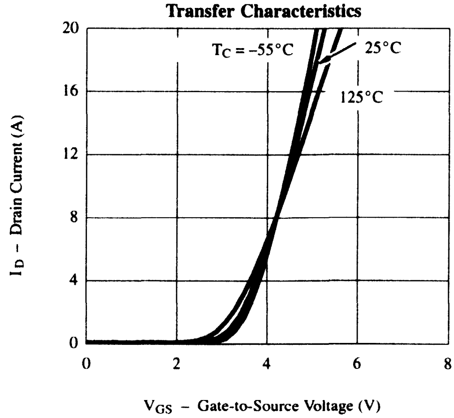
Specifications ($T_J = 25°C$ Unless Otherwise Noted)

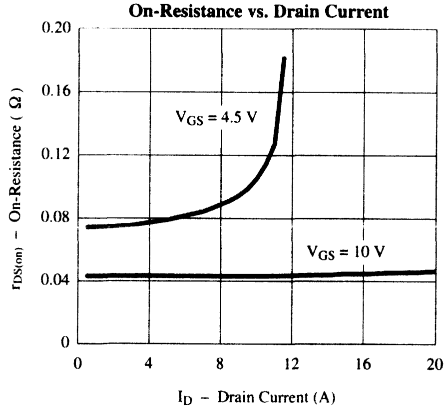
Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Static							
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\ \mu A$	N-Ch	1.0			V
		$V_{DS} = V_{GS}$, $I_D = -250\ \mu A$	P-Ch	-1.0			
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = \pm 20$ V	N-Ch			± 100	nA
			P-Ch			± 100	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30$ V, $V_{GS} = 0$ V	N-Ch			1	µA
		$V_{DS} = -30$ V, $V_{GS} = 0$ V	P-Ch			-1	
		$V_{DS} = 30$ V, $V_{GS} = 0$ V, $T_J = 55°C$	N-Ch			25	
		$V_{DS} = -30$ V, $V_{GS} = 0$ V, $T_J = 55°C$	P-Ch			-25	
On-State Drain Current[b]	$I_{D(on)}$	$V_{DS} \geq 5$ V, $V_{GS} = 10$ V	N-Ch	15			A
		$V_{DS} \geq -5$ V, $V_{GS} = -10$ V	P-Ch	-15			
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	$V_{GS} = 10$ V, $I_D = 3.9$ A	N-Ch		0.043	0.065	Ω
		$V_{GS} = -10$ V, $I_D = 2.5$ A	P-Ch		0.066	0.085	
		$V_{GS} = 4.5$ V, $I_D = 3.1$ A	N-Ch		0.075	0.095	
		$V_{GS} = -4.5$ V, $I_D = 1.8$ A	P-Ch		0.125	0.19	
Forward Transconductance[b]	g_{fs}	$V_{DS} = 15$ V, $I_D = 3.9$ A	N-Ch		7		S
		$V_{DS} = -15$ V, $I_D = -2.5$ A	P-Ch		5		
Diode Forward Voltage[b]	V_{SD}	$I_S = 1.25$ A, $V_{GS} = 0$ V	N-Ch		0.8	1.2	V
		$I_S = -1.25$ A, $V_{GS} = 0$ V	P-Ch		0.8	-1.2	
Dynamic[a]							
Total Gate Charge	Q_g	N-Channel $V_{DS} = 10$ V, $V_{GS} = 10$ V, $I_D = 3.9$ A; P-Channel $V_{DS} = -10$ V, $V_{GS} = -10$ V, $I_D = -2.5$ A	N-Ch		9.8	15	nC
			P-Ch		8.7	15	
Gate-Source Charge	Q_{gs}		N-Ch		2.1		
			P-Ch		1.9		
Gate-Drain Charge	Q_{gd}		N-Ch		1.6		
			P-Ch		1.3		
Turn-On Delay Time	$t_{d(on)}$	N-Channel $V_{DD} = 10$ V, $R_L = 10\ \Omega$, $I_D \cong 1$ A, $V_{GEN} = 10$ V, $R_G = 6\ \Omega$; P-Channel $V_{DD} = -10$ V, $R_L = 10\ \Omega$, $I_D \cong -1$ A, $V_{GEN} = -10$ V, $R_G = 6\ \Omega$	N-Ch		9	15	ns
			P-Ch		7	15	
Rise Time	t_r		N-Ch		6	18	
			P-Ch		9	18	
Turn-Off Delay Time	$t_{d(off)}$		N-Ch		18	27	
			P-Ch		14	27	
Fall Time	t_f		N-Ch		6	15	
			P-Ch		8	15	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 1.25$ A, di/dt = 100 A/µs	N-Ch		48	80	
		$I_F = -1.25$ A, di/dt = 100 A/µs	P-Ch		46	80	

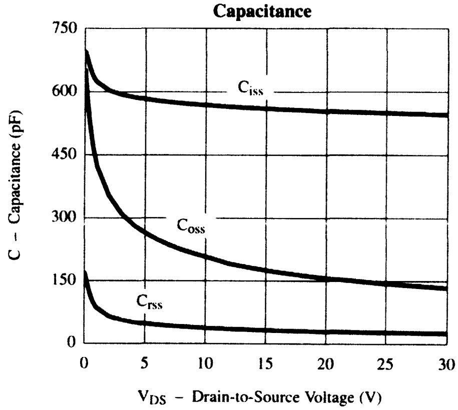
Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

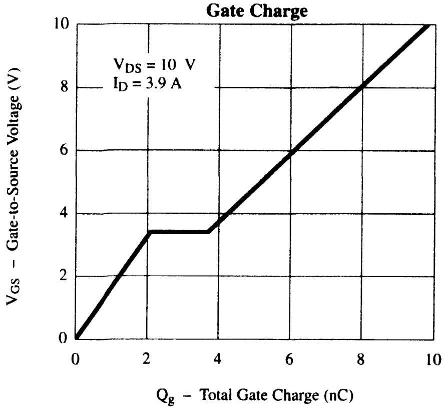
Typical Characteristics (25 °C Unless Noted) N-Channel

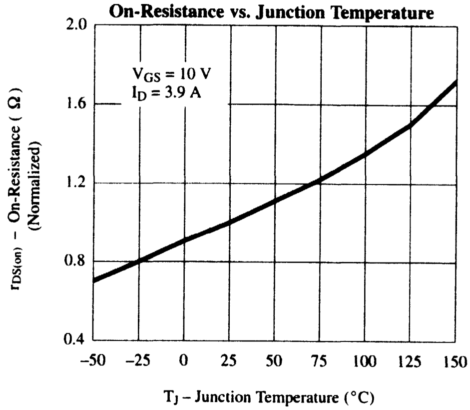






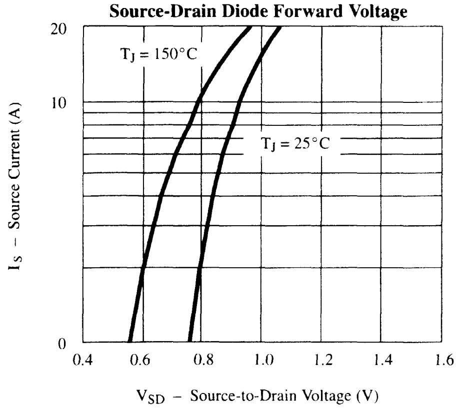




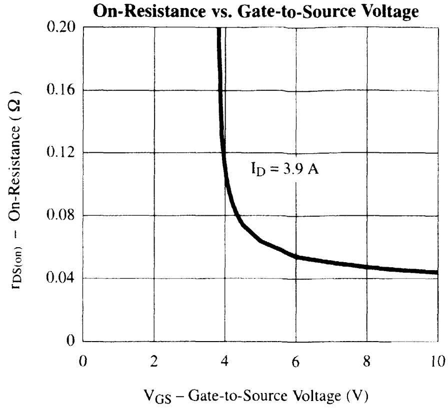


Typical Characteristics (25°C Unless Noted) N-Channel

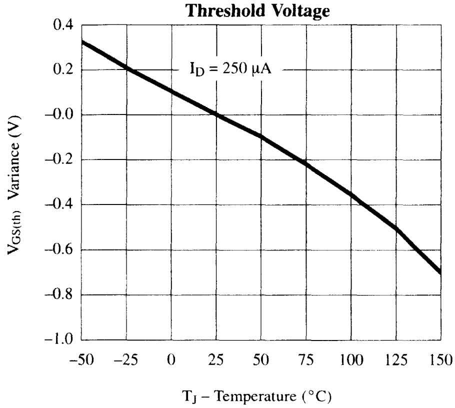
Source-Drain Diode Forward Voltage



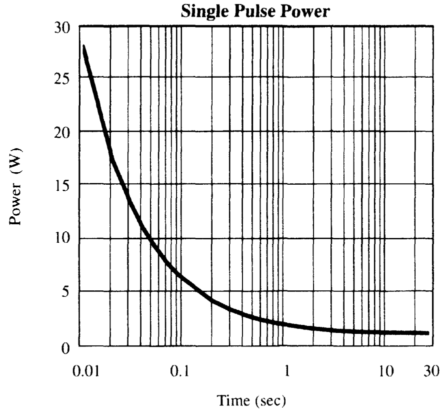
On-Resistance vs. Gate-to-Source Voltage



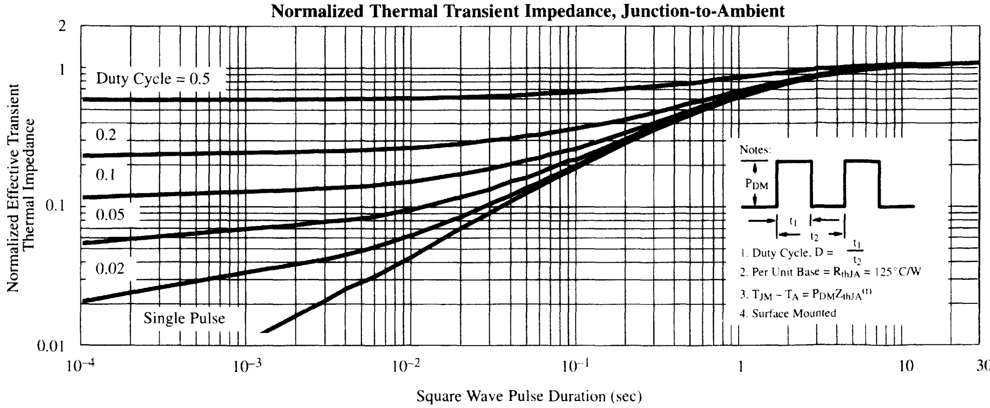
Threshold Voltage



Single Pulse Power

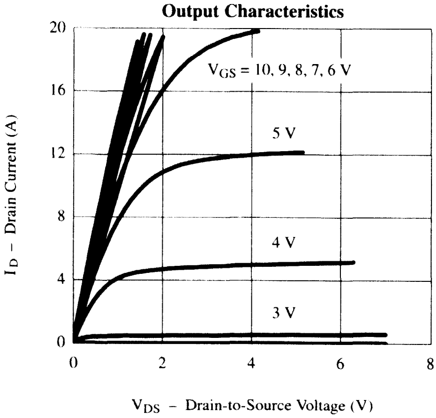


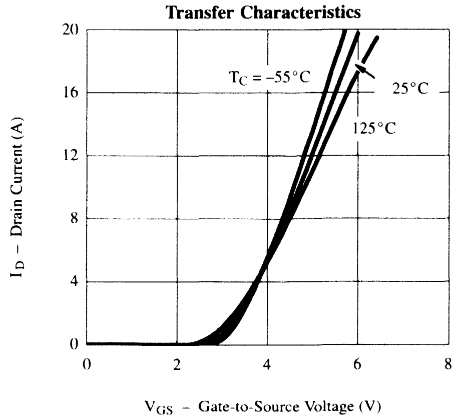
Normalized Thermal Transient Impedance, Junction-to-Ambient

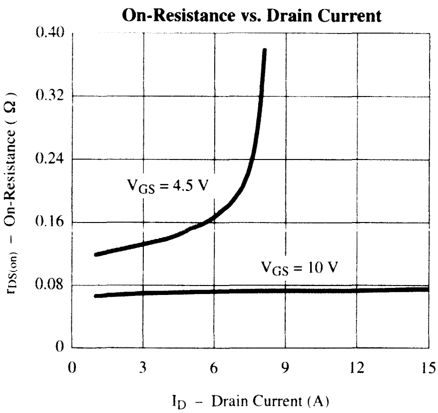


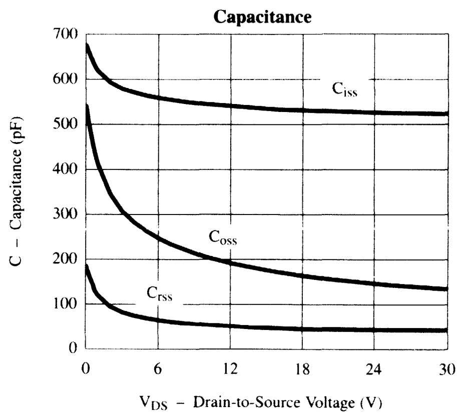
New Product

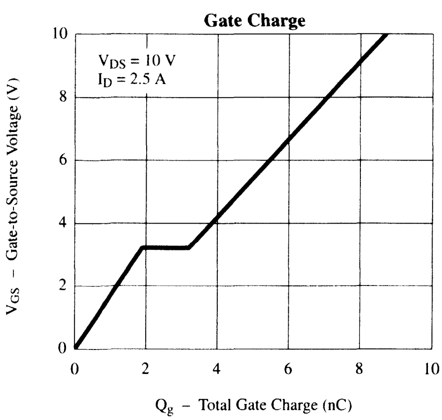
Typical Characteristics (25°C Unless Noted) P-Channel

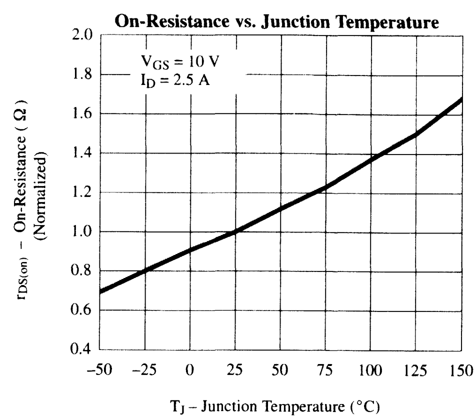








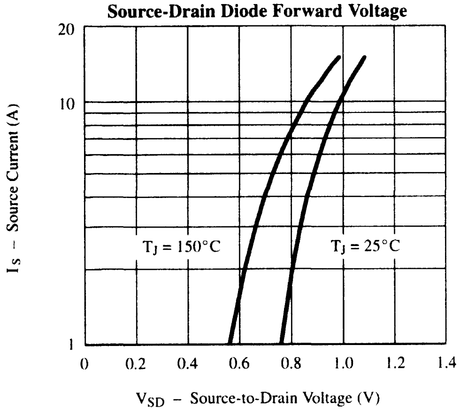




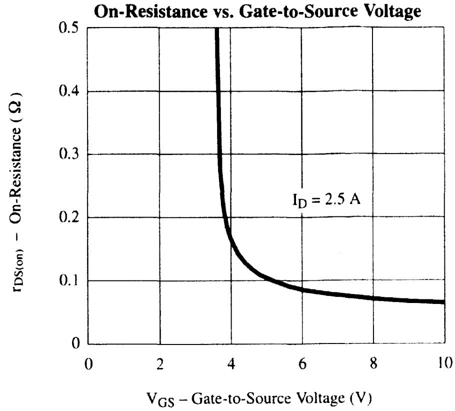
New Product

Typical Characteristics (25 °C Unless Noted) — P-Channel

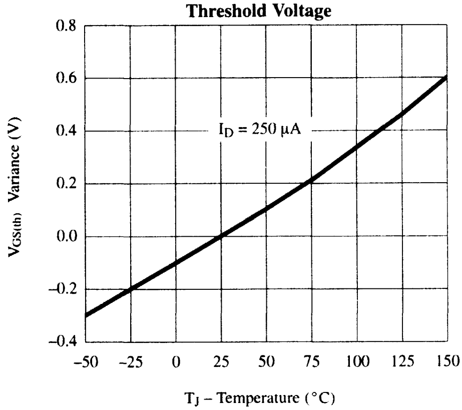
Source-Drain Diode Forward Voltage



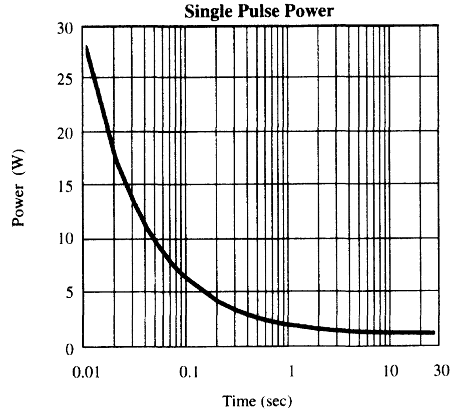
On-Resistance vs. Gate-to-Source Voltage



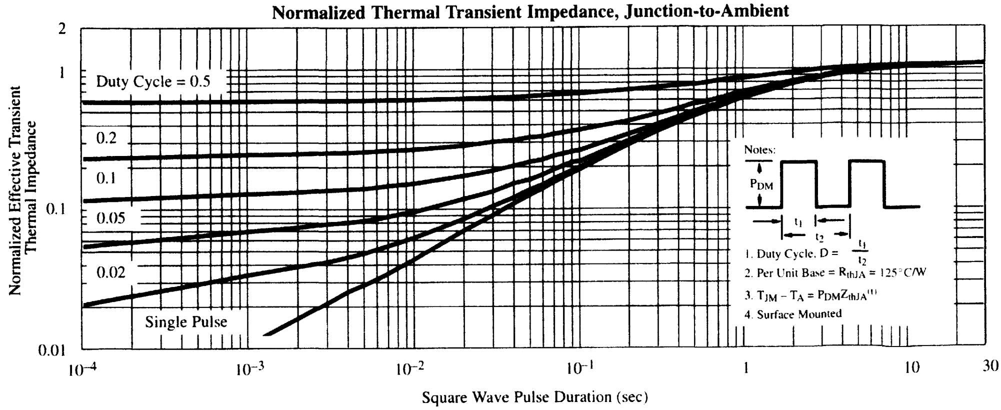
Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient



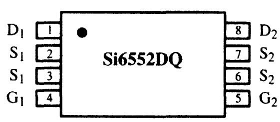
New Product

Dual Enhancement-Mode MOSFET (N- and P-Channel)

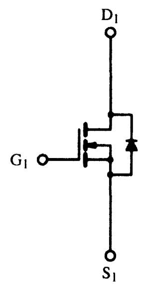
Product Summary

	V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
N-Channel	20	0.08 @ V_{GS} = 4.5 V	± 2.8
		0.11 @ V_{GS} = 2.5 V	± 2.1
P-Channel	–12	0.1 @ V_{GS} = –4.5 V	± 2.5
		0.18 @ V_{GS} = –2.5 V	± 1.9

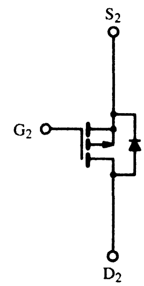
TSSOP-8



Top View



N-Channel MOSFET



P-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage		V_{DS}	20	–12	V
Gate-Source Voltage		V_{GS}	± 8		
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	± 2.8	± 2.5	A
	T_A = 70°C		± 2.3	± 2.0	
Pulsed Drain Current		I_{DM}	± 20		
Continuous Source Current (Diode Conduction)[a]		I_S	1.0	–1.0	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	1.0		W
	T_A = 70°C		0.64		
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150		°C

Thermal Resistance Ratings

Parameter	Symbol	N- or P-Channel	Unit
Maximum Junction-to-Ambient[a]	R_{thJA}	125	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70175.

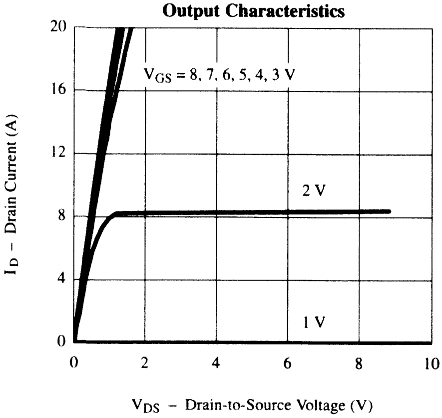
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Static							
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 µA	N-Ch	0.6			V
		$V_{DS} = V_{GS}$, I_D = –250 µA	P-Ch	–0.6			
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 8 V				± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V	N-Ch			1	µA
		V_{DS} = –12 V, V_{GS} = 0 V	P-Ch			–1	
		V_{DS} = 20 V, V_{GS} = 0 V, T_J = 70°C	N-Ch			5	
		V_{DS} = –12 V, V_{GS} = 0 V, T_J = 70°C	P-Ch			–5	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 4.5 V	N-Ch	10			A
		V_{DS} = –5 V, V_{GS} = –4.5 V	P-Ch	–10			
		V_{DS} = 5 V, V_{GS} = 2.5 V	N-Ch	4			
		V_{DS} = –5 V, V_{GS} = –2.5 V	P-Ch	–4			
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = 4.5 V, I_D = 2.8 A	N-Ch			0.08	Ω
		V_{GS} = –4.5 V, I_D = 2.5 A	P-Ch			0.1	
		V_{GS} = 2.5 V, I_D = 2.1 A	N-Ch			0.11	
		V_{GS} = –2.5 V, I_D = 1.9 A	P-Ch			0.18	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 2.8 A	N-Ch		12		S
		V_{DS} = –9 V, I_D = –2.5 A	P-Ch		7		
Diode Forward Voltage[a]	V_{SD}	I_S = 1.0 A, V_{GS} = 0 V	N-Ch			1.2	V
		I_S = –1.0 A, V_{GS} = 0 V	P-Ch			–1.2	
Dynamic[b]							
Total Gate Charge	Q_g	N-Channel V_{DS} = 10 V, V_{GS} = 4.5 V, I_D = 2.8 A P-Channel V_{DS} = –6 V, V_{GS} = –4.5 V, I_D = –2.5 A	N-Ch		16	40	nC
			P-Ch		9	20	
Gate-Source Charge	Q_{gs}		N-Ch		3		
			P-Ch		2		
Gate-Drain Charge	Q_{gd}		N-Ch		6		
			P-Ch		3		
Turn-On Delay Time	$t_{d(on)}$	N-Channel V_{DD} = 10 V, R_L = 10 Ω I_D ≅ 1 A, V_{GEN} = 4.5 V, R_G = 6 Ω P-Channel V_{DD} = –6 V, R_L = 6 Ω I_D ≅ –1 A, V_{GEN} = –4.5 V, R_G = 6 Ω	N-Ch		37	60	ns
			P-Ch		21	40	
Rise Time	t_r		N-Ch		66	100	
			P-Ch		35	70	
Turn-Off Delay Time	$t_{d(off)}$		N-Ch		56	100	
			P-Ch		43	80	
Fall Time	t_f		N-Ch		57	100	
			P-Ch		22	40	
Source-Drain Reverse Recovery Time	t_{rr}	N-Channel—I_F = 1.0 A, di/dt = 100 A/µs	N-Ch		26	70	
		P-Channel—I_F = –1.0 A, di/dt = 100 A/µs	P-Ch		35	70	

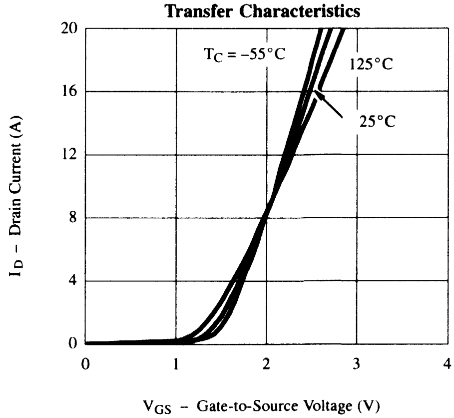
Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

Typical Characteristics (25°C Unless Noted) N-Channel

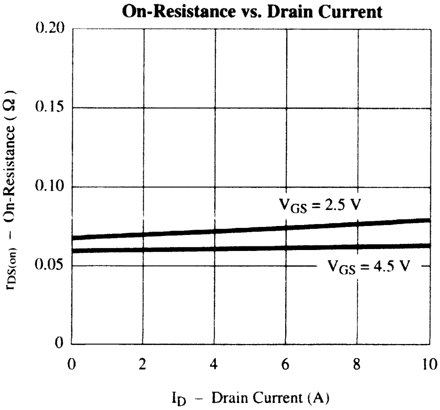
Output Characteristics



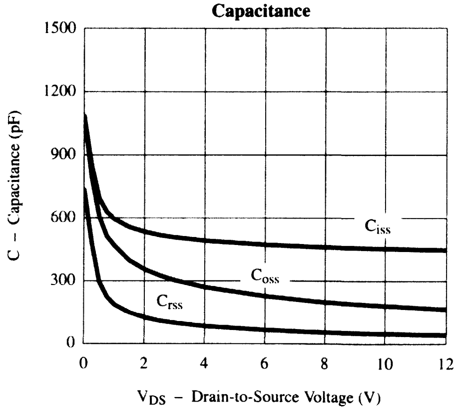
Transfer Characteristics



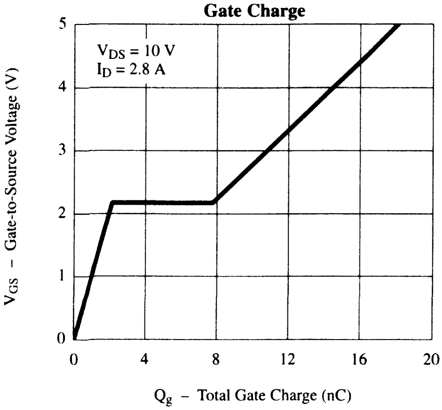
On-Resistance vs. Drain Current



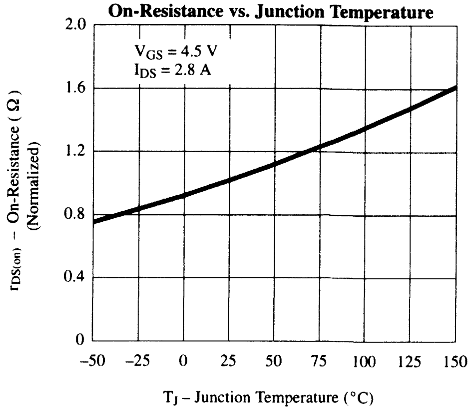
Capacitance



Gate Charge



On-Resistance vs. Junction Temperature



2

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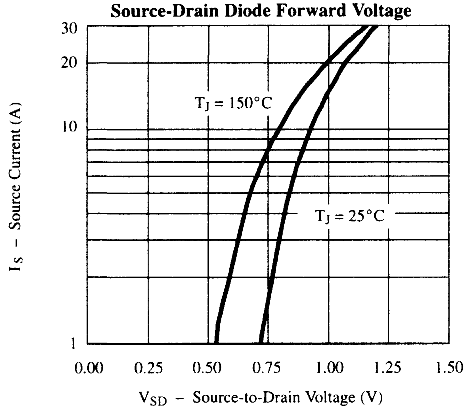
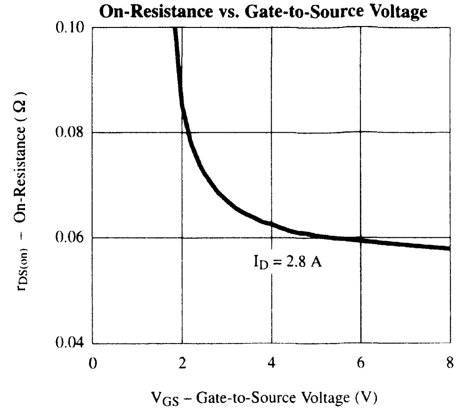
Typical Characteristics (25°C Unless Noted) N-Channel

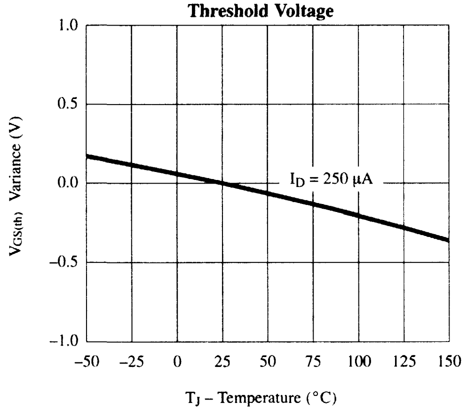
Source-Drain Diode Forward Voltage



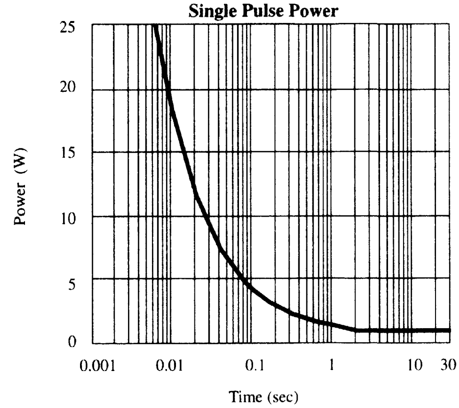
On-Resistance vs. Gate-to-Source Voltage



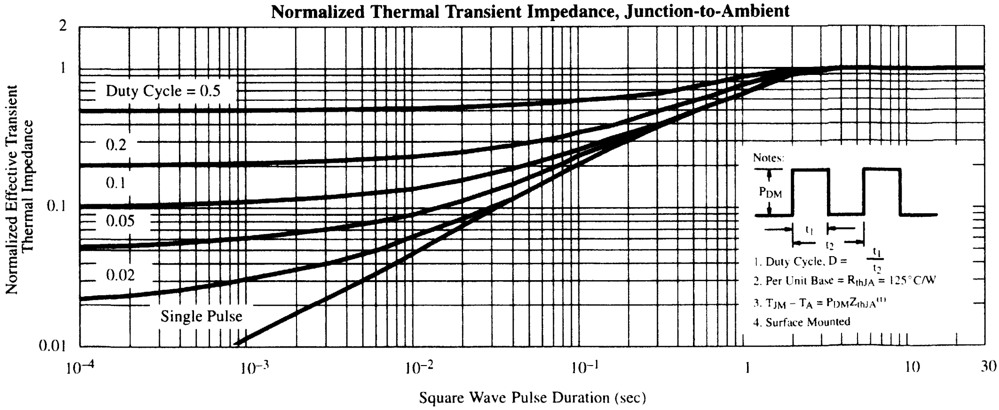
Threshold Voltage



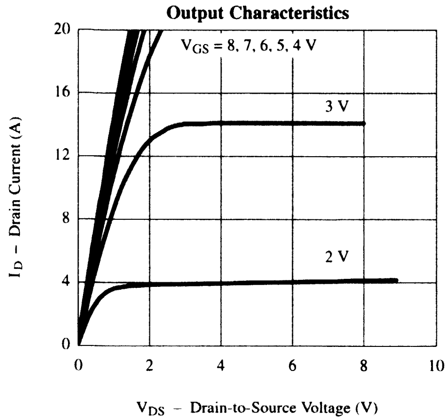
Single Pulse Power

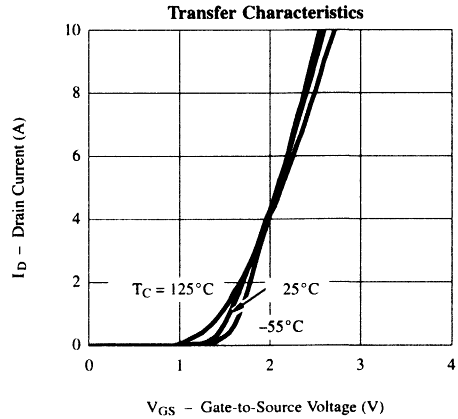


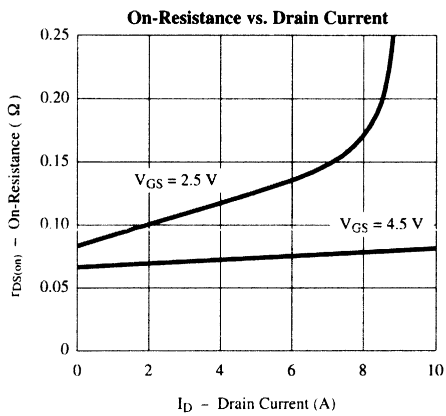
Normalized Thermal Transient Impedance, Junction-to-Ambient

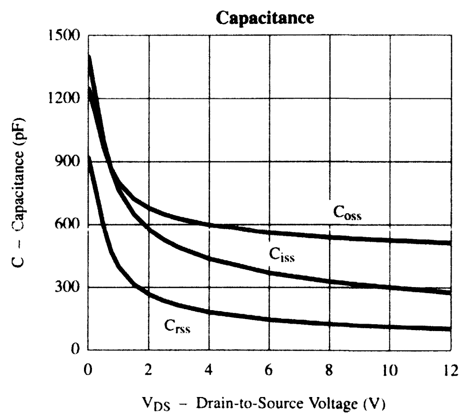


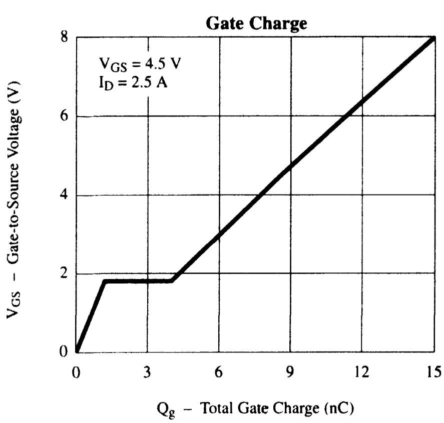
Typical Characteristics (25°C Unless Noted) P-Channel

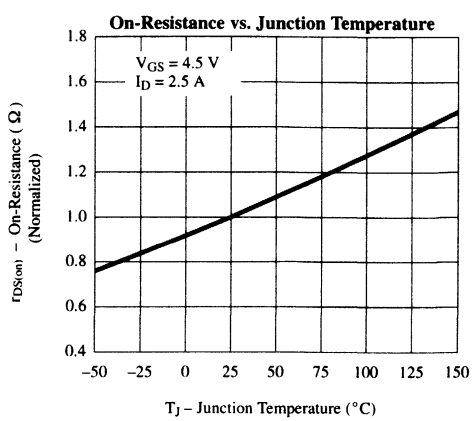




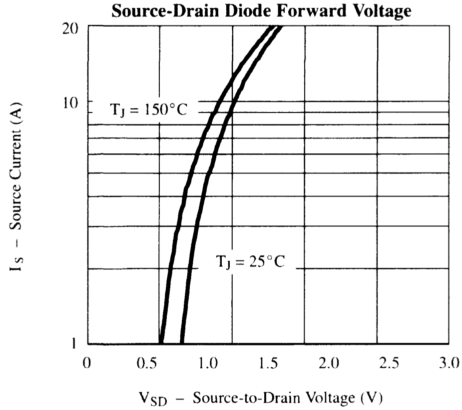


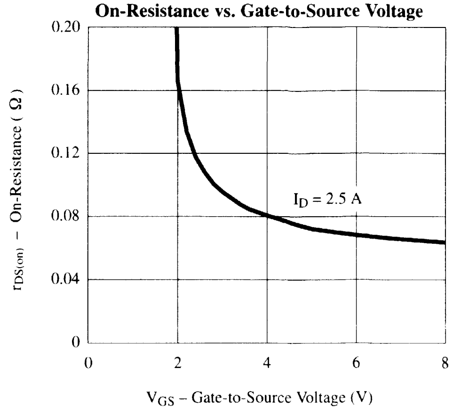


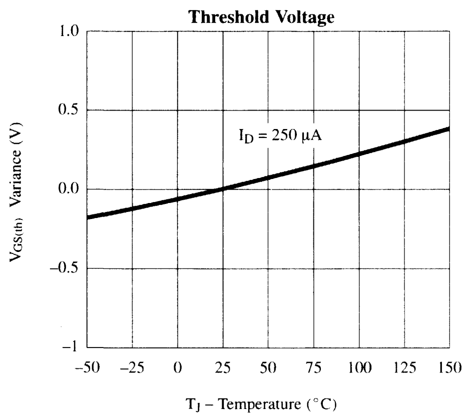


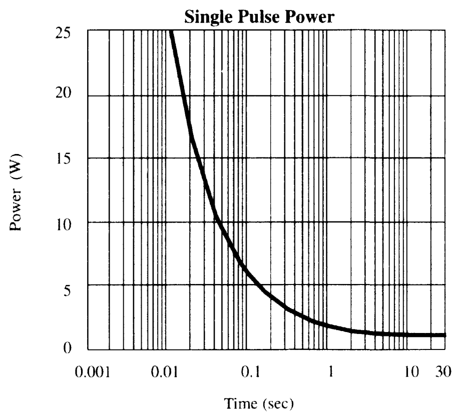


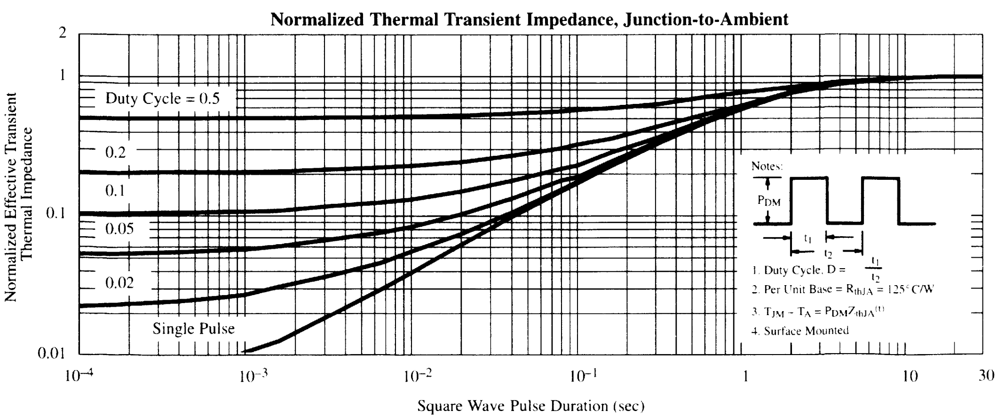
Typical Characteristics (25°C Unless Noted) P-Channel











Dual N-Channel 2.5-V (G-S) Rated MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
20	0.05 @ V_{GS} = 4.5 V	± 3.4
	0.06 @ V_{GS} = 3.0 V	± 3.1
	0.08 @ V_{GS} = 2.5 V	± 2.7

2.5-V Rated

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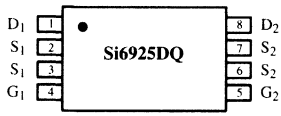
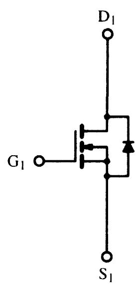
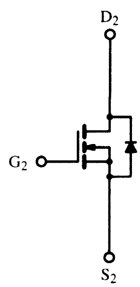


Top View



N-Channel MOSFET



N-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	± 12	
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	± 3.4	A
	T_A = 70°C		± 2.7	
Pulsed Drain Current (10 µs Pulse Width)		I_{DM}	± 30	
Continuous Source Current (Diode Conduction)[a]		I_S	1.25	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	1	W
	T_A = 70°C		0.64	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient[a]	R_{thJA}	125	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 10 sec.

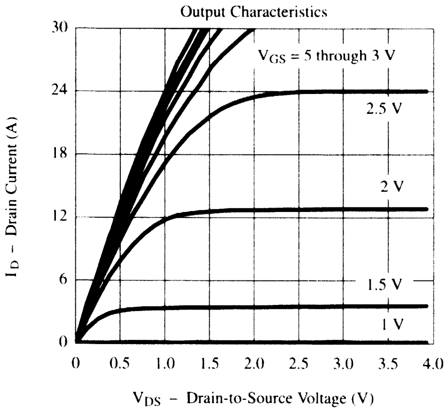
Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70632.

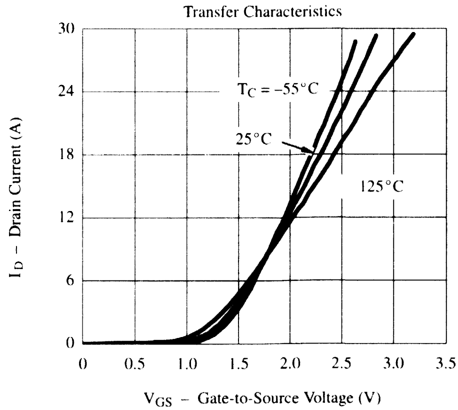
Specifications (T_J = 25°C Unless Otherwise Noted)

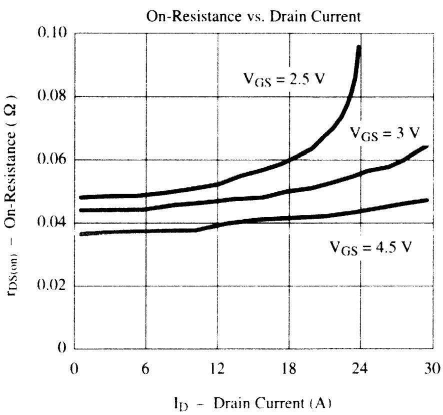
Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\ \mu A$	0.5			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = \pm 12$ V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20$ V, $V_{GS} = 0$ V			1	µA
		$V_{DS} = 16$ V, $V_{GS} = 0$ V, $T_J = 70°C$			5	
On-State Drain Current[b]	$I_{D(on)}$	$V_{DS} \geq 5$ V, $V_{GS} = 4.5$ V	10			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	$V_{GS} = 4.5$ V, $I_D = 3.4$ A		0.038	0.05	Ω
		$V_{GS} = 3.0$ V, $I_D = 3.1$ A		0.044	0.07	
		$V_{GS} = 2.5$ V, $I_D = 2.7$ A		0.048	0.08	
Forward Transconductance[b]	g_{fs}	$V_{DS} = 10$ V, $I_D = 3.4$ A		18		S
Diode Forward Voltage[b]	V_{SD}	$I_S = 1.25$ A, $V_{GS} = 0$ V		0.7	1.2	V
Dynamic[a]						
Total Gate Charge	Q_g	$V_{DS} = 6$ V, $V_{GS} = 4.5$ V, $I_D = 3.4$ A		7.5	15	nC
Gate-Source Charge	Q_{gs}			1.2		
Gate-Drain Charge	Q_{gd}			1.8		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 6$ V, $R_L = 6\ \Omega$ $I_D \cong 1$ A, $V_{GEN} = 4.5$ V, $R_G = 6\ \Omega$		10	20	ns
Rise Time	t_r			25	50	
Turn-Off Delay Time	$t_{d(off)}$			40	60	
Fall Time	t_f			10	20	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 1.25$ A, di/dt = 100 A/µs		50	90	

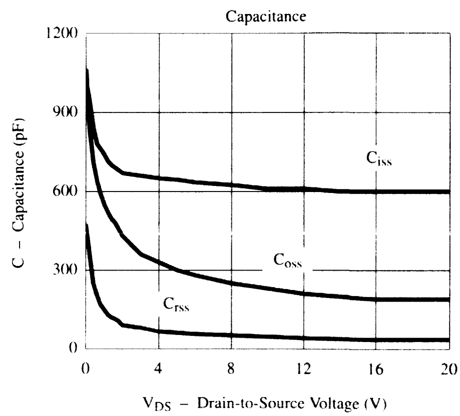
Notes
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

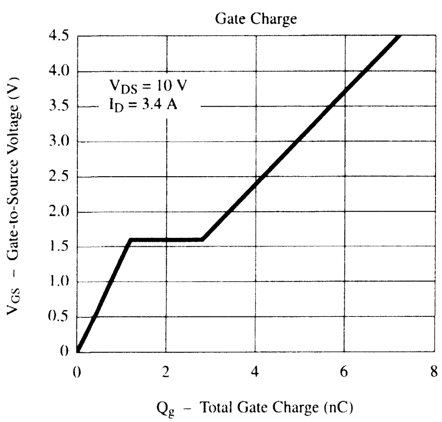
Typical Characteristics (25°C Unless Otherwise Noted)

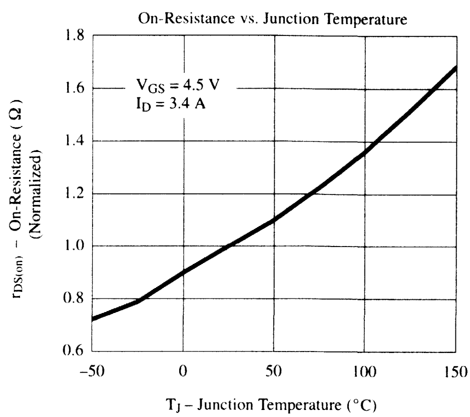






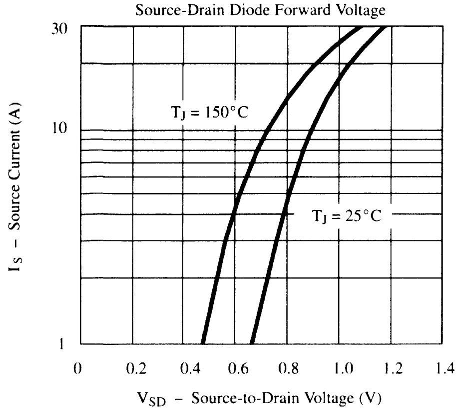




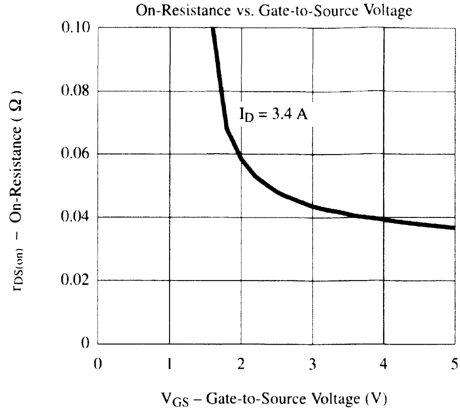


Typical Characteristics (25°C Unless Otherwise Noted)

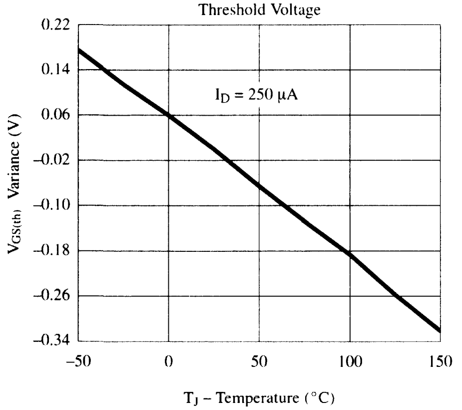
Source-Drain Diode Forward Voltage



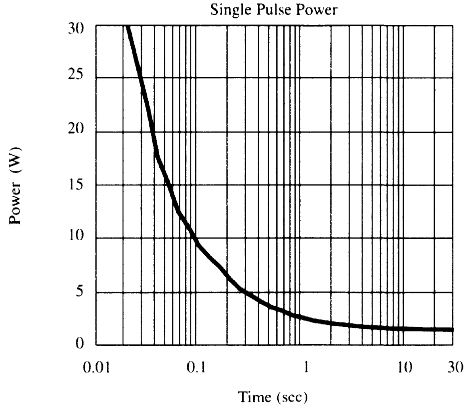
On-Resistance vs. Gate-to-Source Voltage



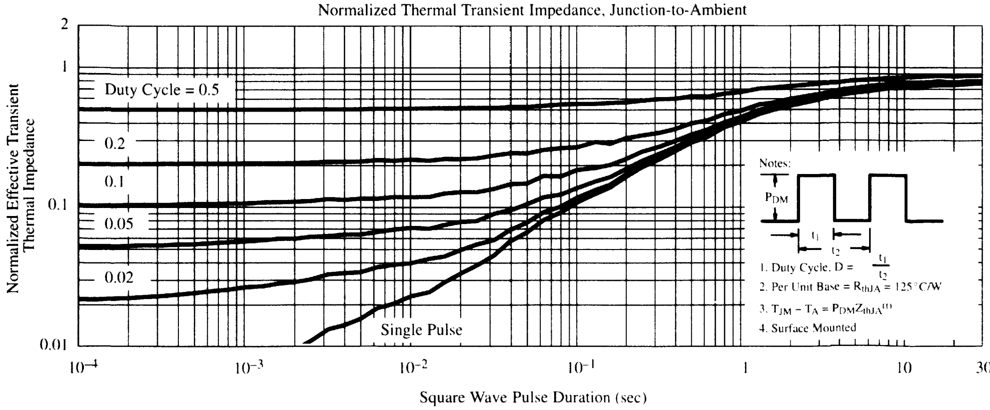
Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient



New Product

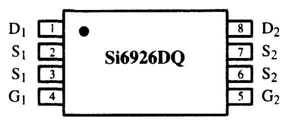
Dual N-Channel 2.5-V (G-S) Rated MOSFET

Product Summary

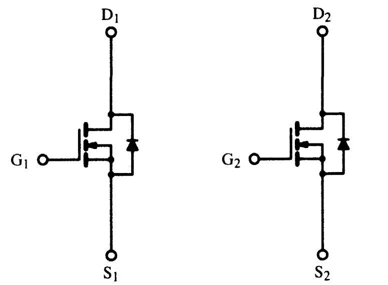
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
20	0.035 @ V_{GS} = 4.5 V	± 4.0
	0.040 @ V_{GS} = 3.0 V	± 3.7
	0.045 @ V_{GS} = 2.5 V	± 3.5

2.5-V Rated

TSSOP-8



Top View



N-Channel MOSFET N-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	± 8	
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	± 4.0	A
	T_A = 70°C		± 3.2	
Pulsed Drain Current		I_{DM}	± 20	
Continuous Source Current (Diode Conduction)[a]		I_S	1.25	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	1.0	W
	T_A = 70°C		0.64	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient[a]	R_{thJA}	125	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70631.

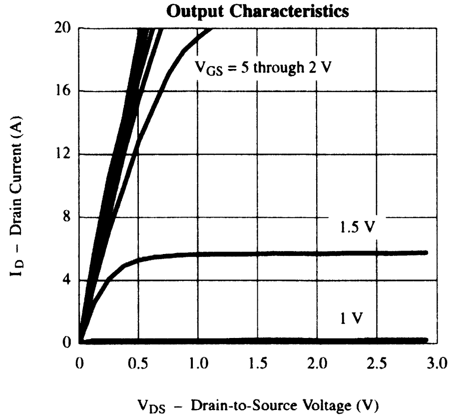
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\ \mu A$	0.5			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = \pm 8$ V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20$ V, $V_{GS} = 0$ V			1	μA
		$V_{DS} = 20$ V, $V_{GS} = 0$ V, $T_J = 55°C$			5	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \geq 5$ V, $V_{GS} = 5$ V	10			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	$V_{GS} = 4.5$ V, $I_D = 4.0$ A		0.028	0.035	Ω
		$V_{GS} = 3.0$ V, $I_D = 3.7$ A		0.031	0.040	
		$V_{GS} = 2.5$ V, $I_D = 3.5$ A		0.033	0.045	
Forward Transconductance[a]	g_{fs}	$V_{DS} = 10$ V, $I_D = 4.0$ A		18		S
Diode Forward Voltage[a]	V_{SD}	$I_S = 1.25$ A, $V_{GS} = 0$ V		0.7	1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	$V_{DS} = 10$ V, $V_{GS} = 4.5$ V, $I_D = 4.0$ A		12	20	nC
Gate-Source Charge	Q_{gs}			1.4		
Gate-Drain Charge	Q_{gd}			3.2		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10$ V, $R_L = 6\ \Omega$ $I_D \cong 1$ A, $V_{GEN} = 10$ V, $R_G = 6\ \Omega$		10	20	ns
Rise Time	t_r			30	50	
Turn-Off Delay Time	$t_{d(off)}$			60	80	
Fall Time	t_f			15	30	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 1.25$ A, di/dt = 100 A/μs		50	90	

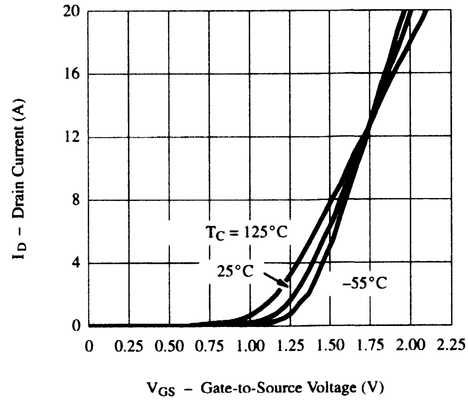
Notes
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

Typical Characteristics (25 °C Unless Otherwise Noted)

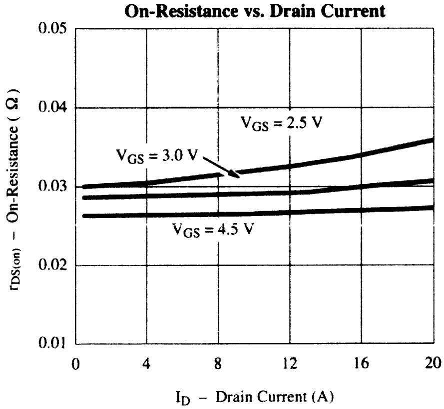
Output Characteristics



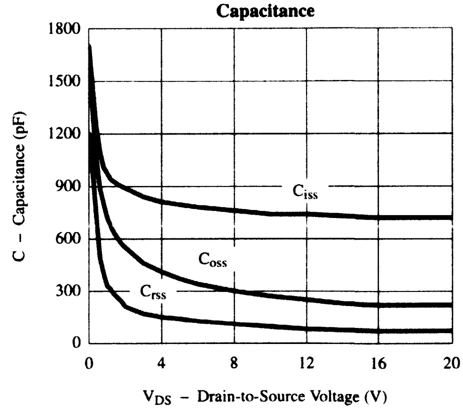
Transfer Characteristics



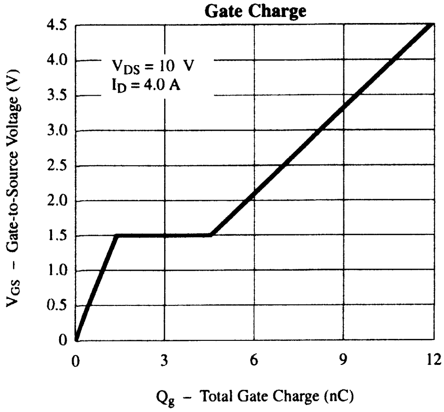
On-Resistance vs. Drain Current



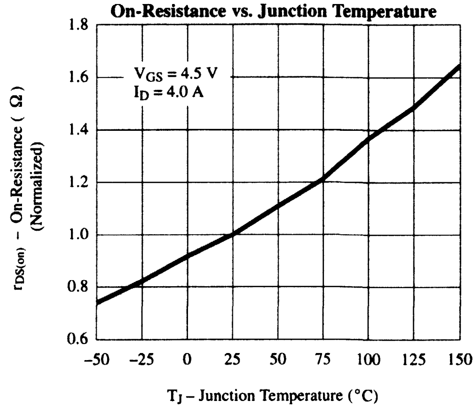
Capacitance



Gate Charge

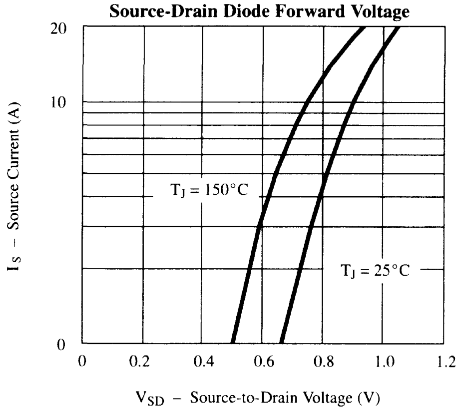


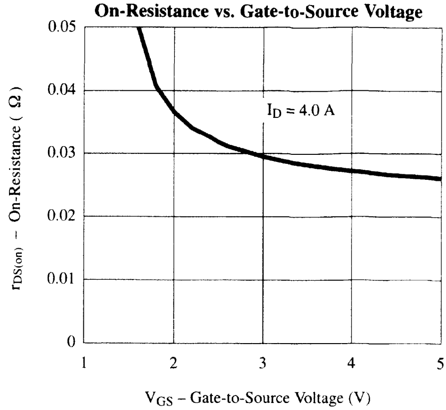
On-Resistance vs. Junction Temperature

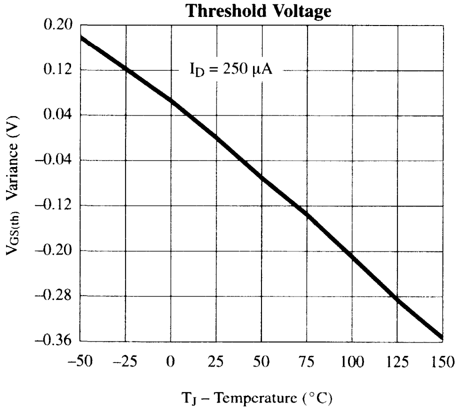


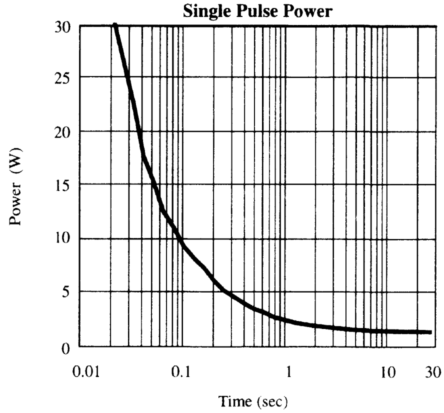
New Product

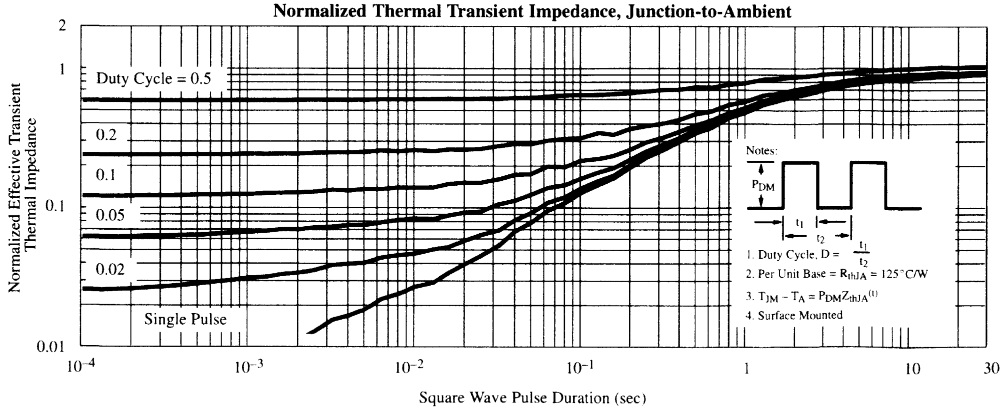
Typical Characteristics (25 °C Unless Otherwise Noted)









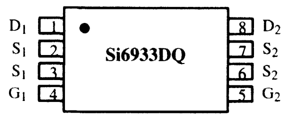


Dual P-Channel 30-V (D-S) Rated MOSFET

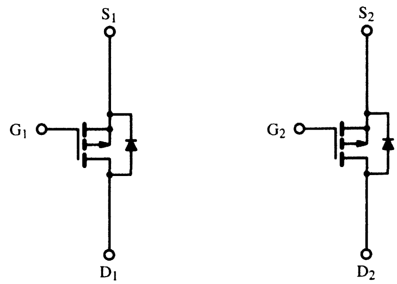
Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
–30	0.045 @ V_{GS} = –10 V	± 3.5
	0.085 @ V_{GS} = –4.5 V	± 2.5

TSSOP-8



Top View



P-Channel MOSFET   P-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	–30	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	± 3.5	A
	T_A = 70°C		± 2.8	
Pulsed Drain Current		I_{DM}	± 20	
Continuous Source Current (Diode Conduction)[a]		I_S	–1.25	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	1.0	W
	T_A = 70°C		0.64	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient[a]	R_{thJA}	125	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70640.

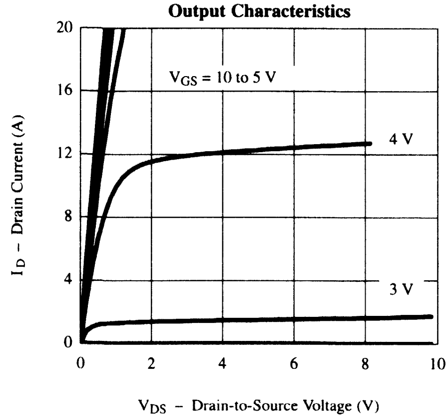
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250\ \mu A$	−1.0			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = \pm 20$ V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -30$ V, $V_{GS} = 0$ V			−1	µA
		$V_{DS} = -30$ V, $V_{GS} = 0$ V, $T_J = 55°C$			−25	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \geq -5$ V, $V_{GS} = -10$ V	−15			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	$V_{GS} = -10$ V, $I_D = 3.5$ A		0.035	0.045	Ω
		$V_{GS} = -4.5$ V, $I_D = 2.5$ A		0.062	0.085	
Forward Transconductance[a]	g_{fs}	$V_{DS} = -15$ V, $I_D = -3.5$ A		7.2		S
Diode Forward Voltage[a]	V_{SD}	$I_S = -1.25$ A, $V_{GS} = 0$ V		−0.77	−1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	$V_{DS} = -15$ V, $V_{GS} = -10$ V, $I_D = -3.5$ A		17	30	nC
Gate-Source Charge	Q_{gs}			4.4		
Gate-Drain Charge	Q_{gd}			3.1		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -15$ V, $R_L = 15\ \Omega$ $I_D \cong -1$ A, $V_{GEN} = -10$ V, $R_G = 6\ \Omega$		13	20	ns
Rise Time	t_r			10	20	
Turn-Off Delay Time	$t_{d(off)}$			33	60	
Fall Time	t_f			10	20	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -1.25$ A, di/dt = 100 A/µs		30	60	

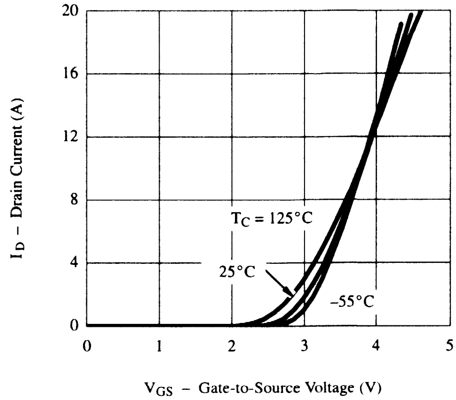
Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

Typical Characteristics (25°C Unless Noted)

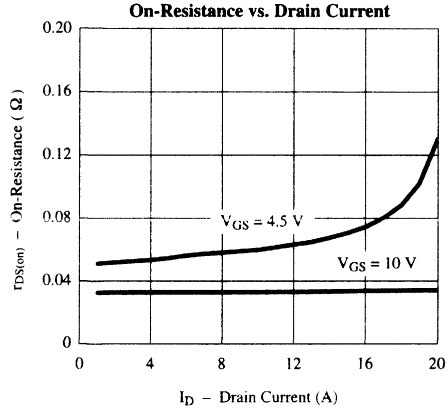
Output Characteristics



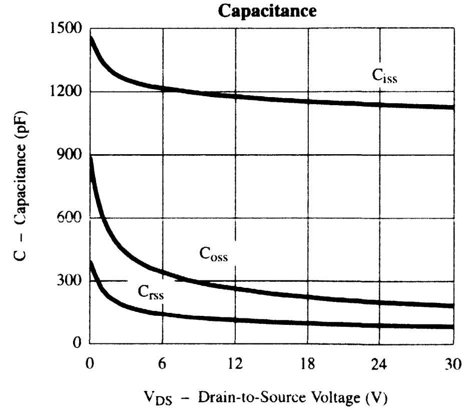
Transfer Characteristics



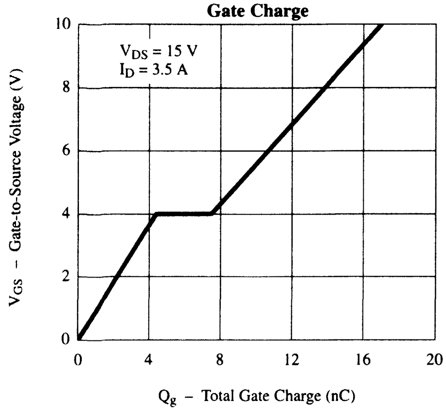
On-Resistance vs. Drain Current



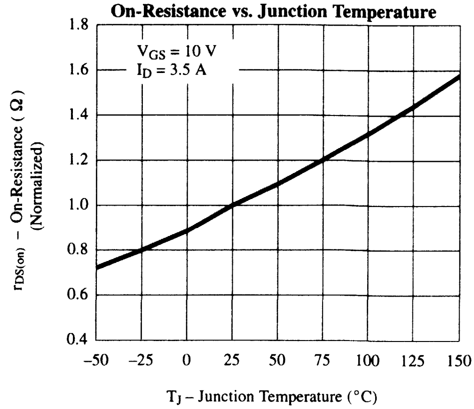
Capacitance



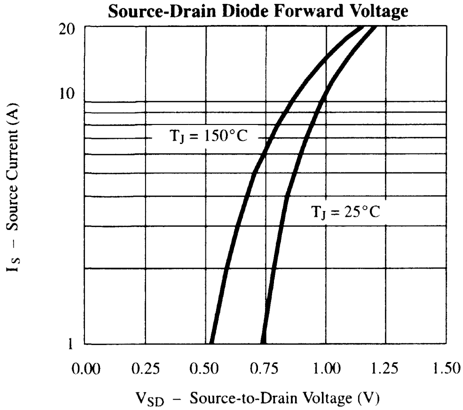
Gate Charge

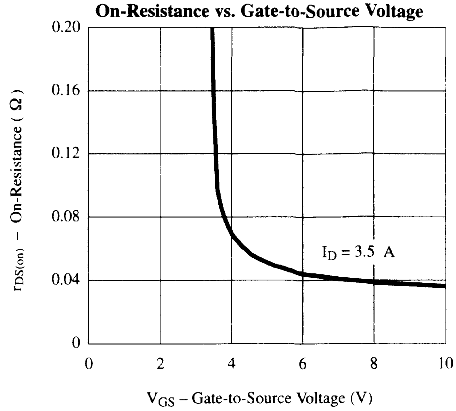


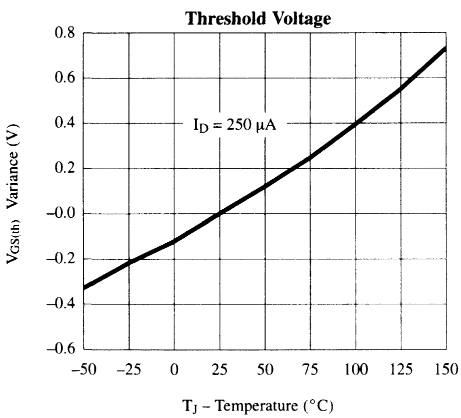
On-Resistance vs. Junction Temperature

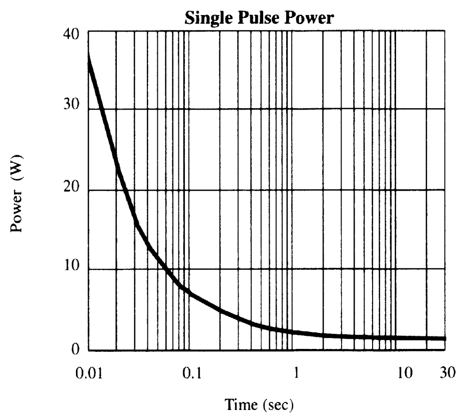


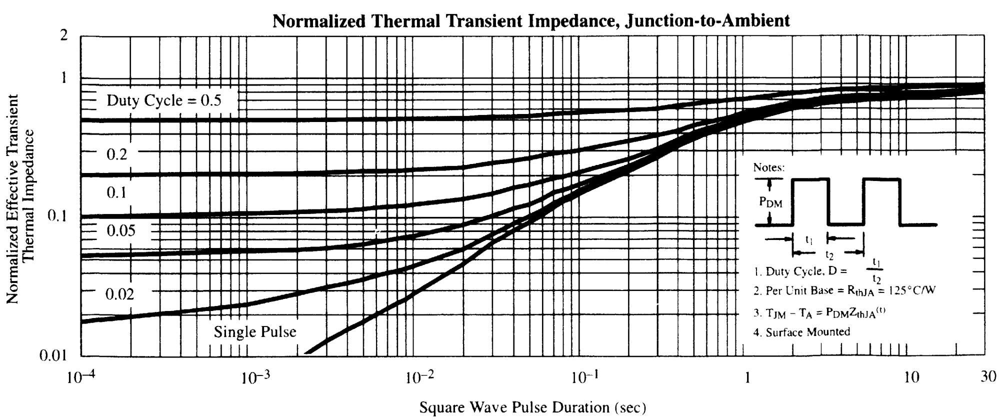
Typical Characteristics (25 °C Unless Noted)









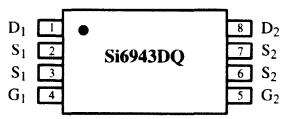


Dual P-Channel Enhancement-Mode MOSFET

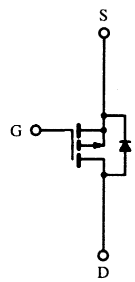
Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
–12	0.10 @ V_{GS} = –4.5 V	± 2.5
	0.18 @ V_{GS} = –2.5 V	± 1.9

TSSOP-8



Top View



P-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	–12	V
Gate-Source Voltage		V_{GS}	± 8	
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	± 2.5	A
	T_A = 70°C		± 2.0	
Pulsed Drain Current		I_{DM}	± 20	
Continuous Source Current (Diode Conduction)[a]		I_S	± 1	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	1.0	W
	T_A = 70°C		0.64	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient[a]	R_{thJA}	125	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70176.
A SPICE Model data sheet is available for this product (FaxBack document #70548).

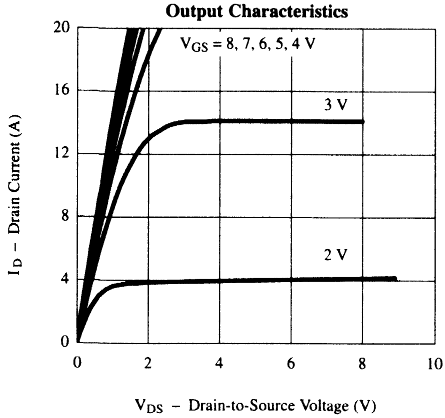
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 µA	–0.6			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±8 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = –12 V, V_{GS} = 0 V			-1	µA
		V_{DS} = –12 V, V_{GS} = 0 V, T_J = 70°C			-5	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} = –5 V, V_{GS} = –4.5 V	–10			A
		V_{DS} = –5 V, V_{GS} = –2.5 V	–4			
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = –4.5 V, I_D = 2.5 A			0.10	Ω
		V_{GS} = –2.5 V, I_D = 1.9 A			0.18	
Forward Transconductance[a]	g_{fs}	V_{DS} = –9 V, I_D = –2.5 A		7		S
Diode Forward Voltage[a]	V_{SD}	I_S = –1.0 A, V_{GS} = 0 V			-1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = –6 V, V_{GS} = –4.5 V, I_D = –2.5 A		9	20	nC
Gate-Source Charge	Q_{gs}			2		
Gate-Drain Charge	Q_{gd}			3		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = –6 V, R_L = 6 Ω I_D ≅ –1.0 A, V_{GEN} = –4.5 V, R_G = 6 Ω		21	40	ns
Rise Time	t_r			35	70	
Turn-Off Delay Time	$t_{d(off)}$			43	80	
Fall Time	t_f			22	40	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = –1.0 A, di/dt = 100 A/µs		35	70	

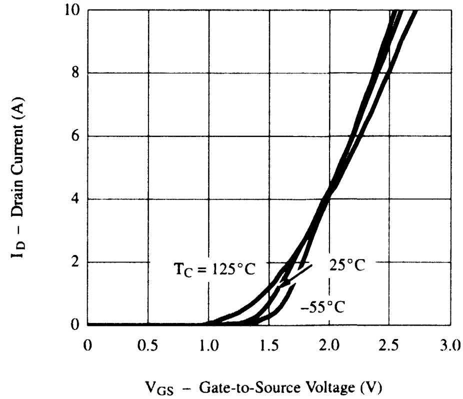
Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

Typical Characteristics (25°C Unless Otherwise Noted)

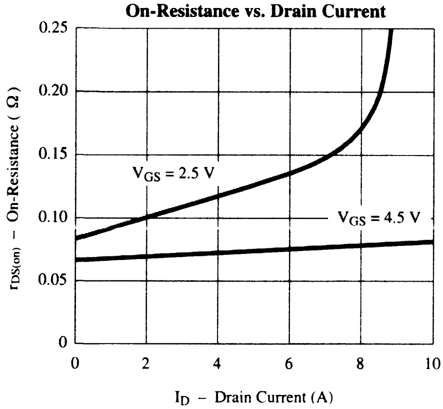
Output Characteristics



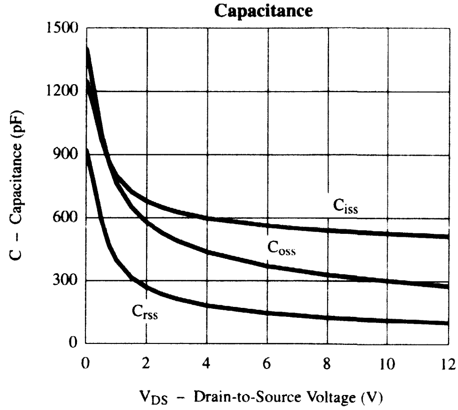
Transfer Characteristics



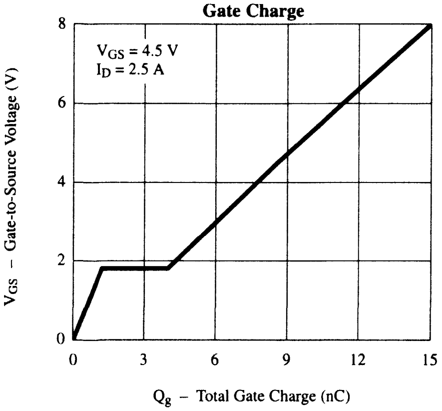
On-Resistance vs. Drain Current



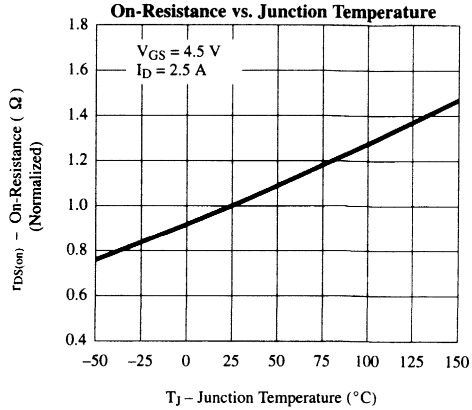
Capacitance



Gate Charge

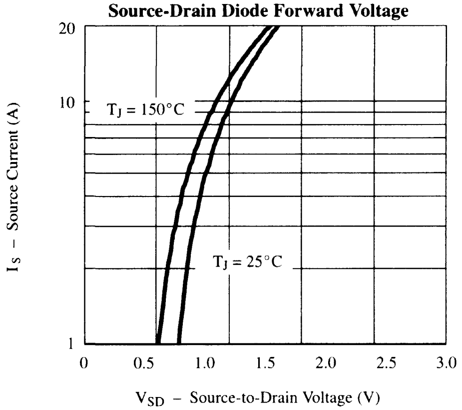


On-Resistance vs. Junction Temperature

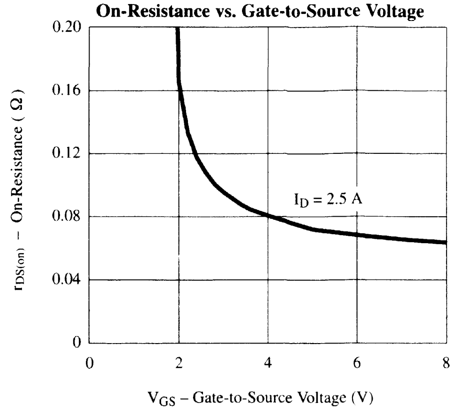


Typical Characteristics (25°C Unless Otherwise Noted)

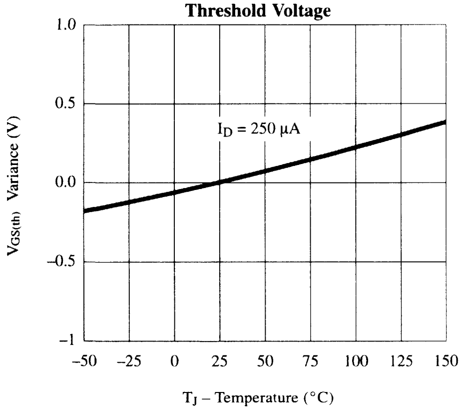
Source-Drain Diode Forward Voltage



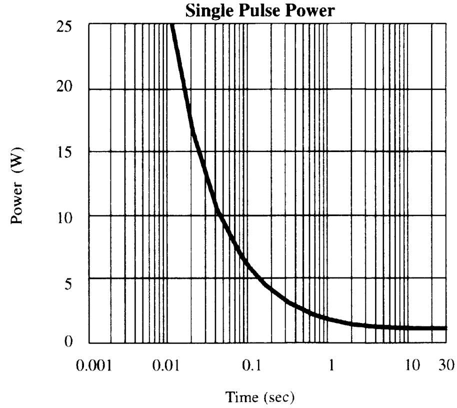
On-Resistance vs. Gate-to-Source Voltage



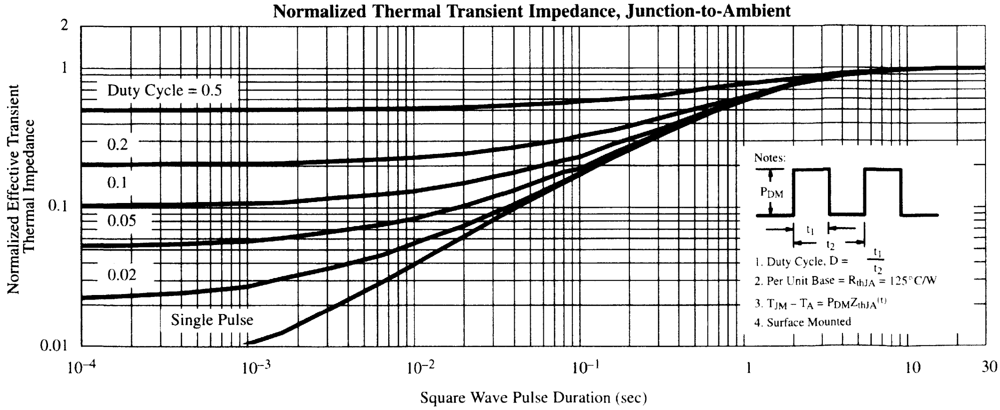
Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient

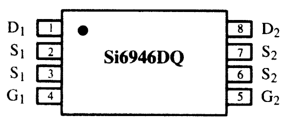


Dual N-Channel Enhancement-Mode MOSFET

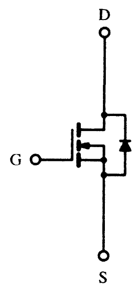
Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
20	0.080 @ V_{GS} = 4.5 V	2.8
	0.110 @ V_{GS} = 2.5 V	2.1

TSSOP-8



Top View



N-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	±8	
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	2.8	A
	T_A = 70°C		2.3	
Pulsed Drain Current		I_{DM}	20	
Continuous Source Current (Diode Conduction)[a]		I_S	1.0	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	1.0	W
	T_A = 70°C		0.64	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient[a]	R_{thJA}	125	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 10 sec.

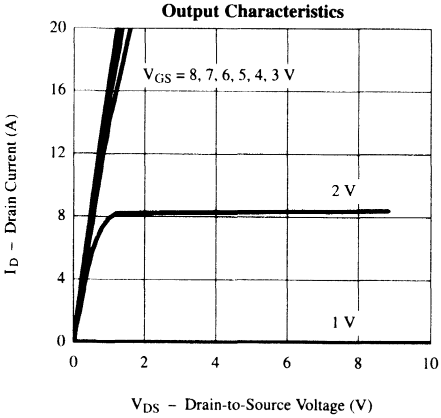
Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70177. A SPICE Model data sheet is available for this product (FaxBack document #70549).

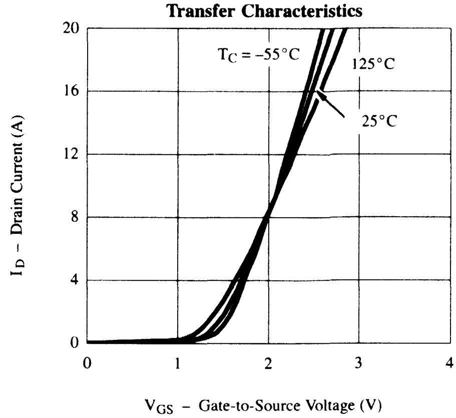
Specifications (T_J = 25°C Unless Otherwise Noted)

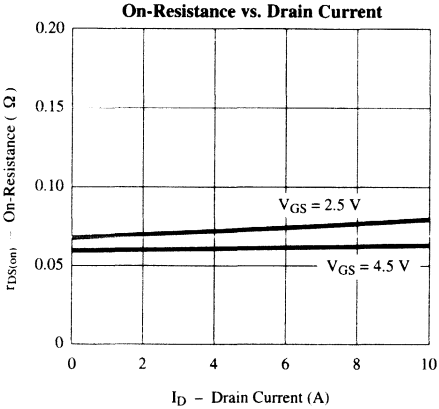
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 µA	0.6			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±8 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V			1	µA
		V_{DS} = 20 V, V_{GS} = 0 V, T_J = 70°C			5	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 4.5 V	±10			A
		V_{DS} = 5 V, V_{GS} = 2.5 V	±4			
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = 4.5 V, I_D = 2.8 A			0.080	Ω
		V_{GS} = 2.5 V, I_D = 2.1 A			0.110	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 2.8 A		12		S
Diode Forward Voltage[a]	V_{SD}	I_S = 1.0 A, V_{GS} = 0 V			1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = 10 V, V_{GS} = 4.5 V, I_D = 2.8 A		16	40	nC
Gate-Source Charge	Q_{gs}			3		
Gate-Drain Charge	Q_{gd}			6		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 10 V, R_L = 10 Ω I_D ≅ 1 A, V_{GEN} = 4.5 V, R_G = 6 Ω		37	60	ns
Rise Time	t_r			66	100	
Turn-Off Delay Time	$t_{d(off)}$			56	100	
Fall Time	t_f			57	100	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 1.0 A, di/dt = 100 A/µs		26	70	

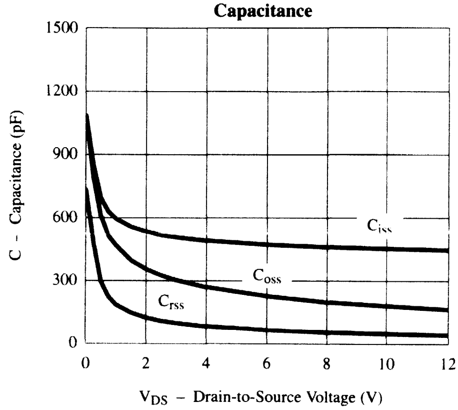
Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

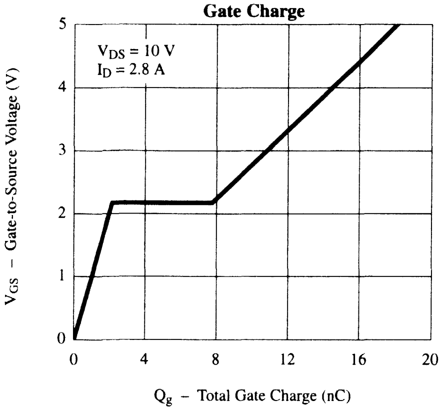
Typical Characteristics (25°C Unless Otherwise Noted)

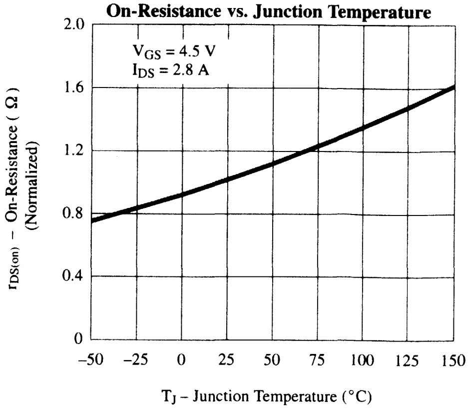




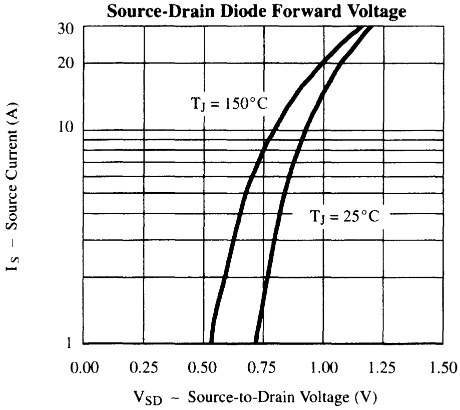


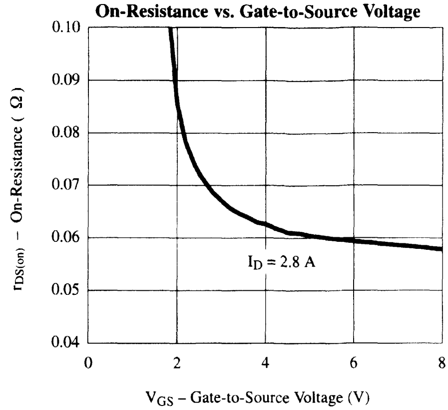


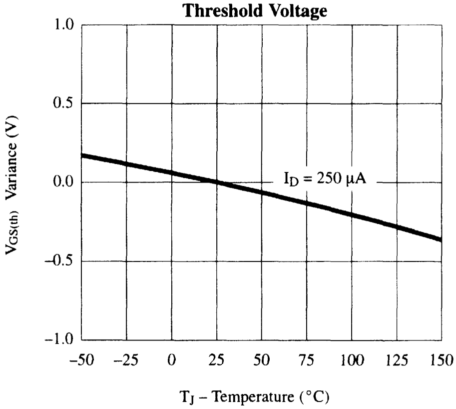


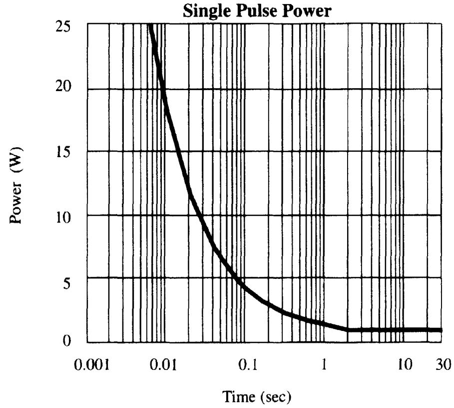


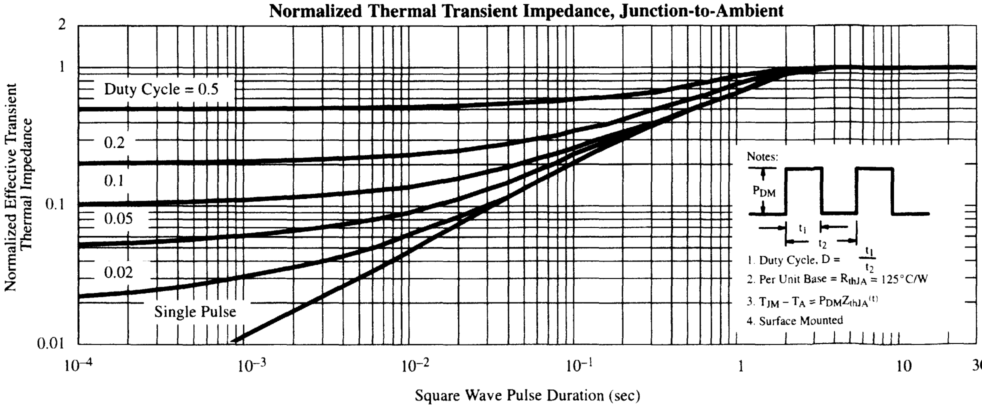
Typical Characteristics (25 °C Unless Otherwise Noted)











TEMIC
Semiconductors

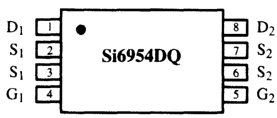
Si6954DQ

Dual N-Channel Enhancement-Mode MOSFET

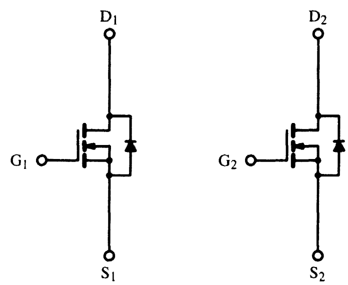
Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
30	0.065 @ V_{GS} = 10 V	± 3.9
	0.095 @ V_{GS} = 4.5 V	± 3.1

TSSOP-8



Top View



N-Channel MOSFET N-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	± 3.9	A
	T_A = 70°C		± 3.1	
Pulsed Drain Current		I_{DM}	± 20	
Continuous Source Current (Diode Conduction)[a]		I_S	1.25	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	1.0	W
	T_A = 70°C		0.64	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient[a]	R_{thJA}	125	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 10 sec.

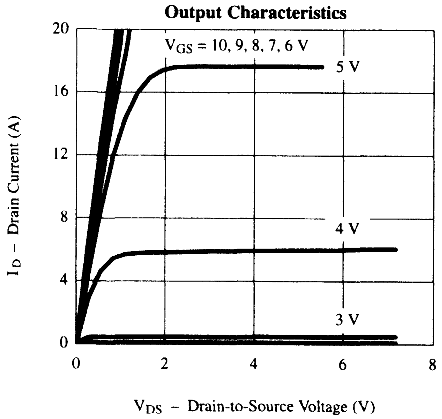
Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70179.

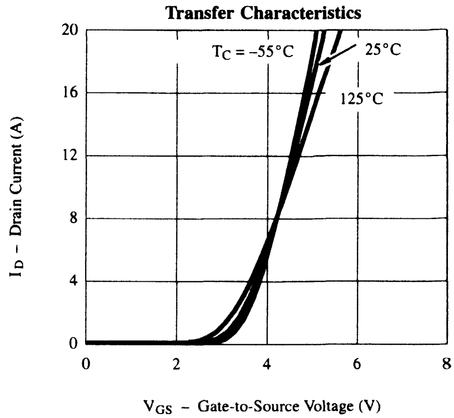
Specifications (T_J = 25°C Unless Otherwise Noted)

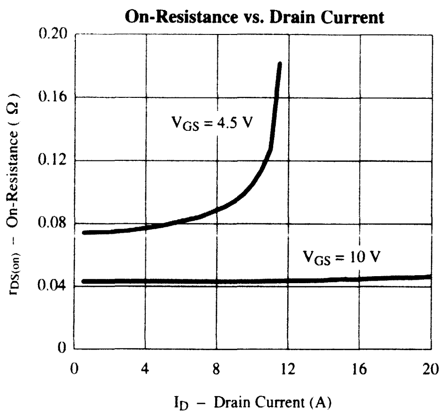
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 μA	1.0			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V			1	μA
		V_{DS} = 30 V, V_{GS} = 0 V, T_J = 55°C			25	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \geq$ 5 V, V_{GS} = 10 V	15			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 3.9 A		0.043	0.065	Ω
		V_{GS} = 4.5 V, I_D = 3.1 A		0.075	0.095	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 3.9 A		7.0		S
Diode Forward Voltage[a]	V_{SD}	I_S = 1.25 A, V_{GS} = 0 V		0.77	1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = 10 V, V_{GS} = 10 V, I_D = 3.9 A		9.8	15	nC
Gate-Source Charge	Q_{gs}			2.1		
Gate-Drain Charge	Q_{gd}			1.6		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 10 V, R_L = 10 Ω $I_D \cong$ 1 A, V_{GEN} = 10 V, R_G = 6 Ω		9	15	ns
Rise Time	t_r			6	12	
Turn-Off Delay Time	$t_{d(off)}$			18	27	
Fall Time	t_f			6	12	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 1.25 A, di/dt = 100 A/μs		48	80	

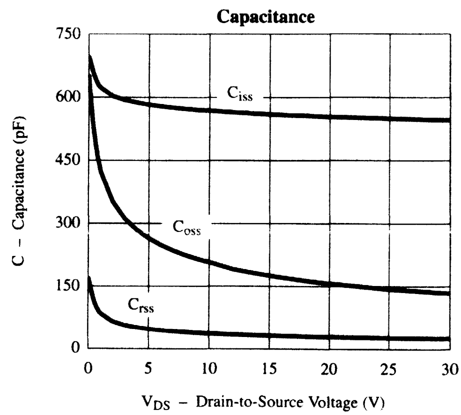
Notes
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

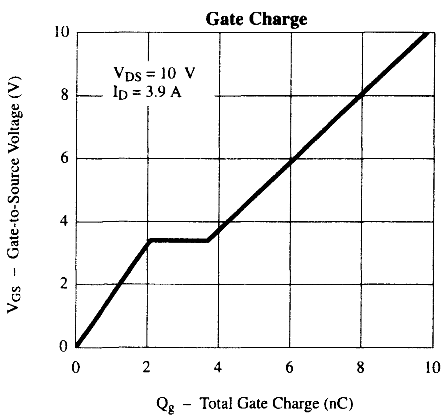
Typical Characteristics (25°C Unless Otherwise Noted)

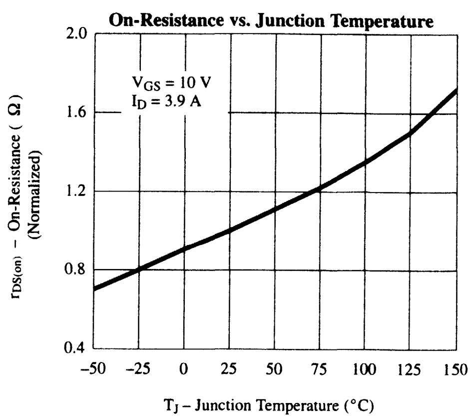




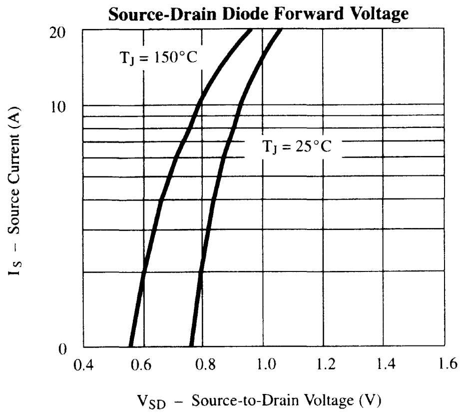


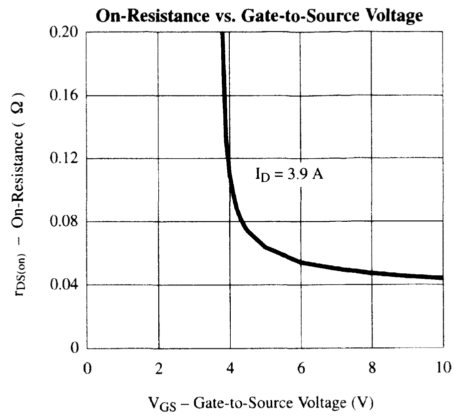


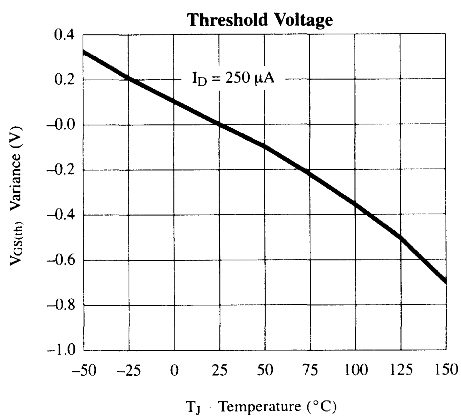


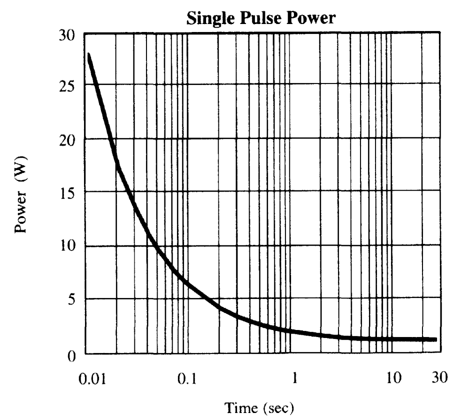


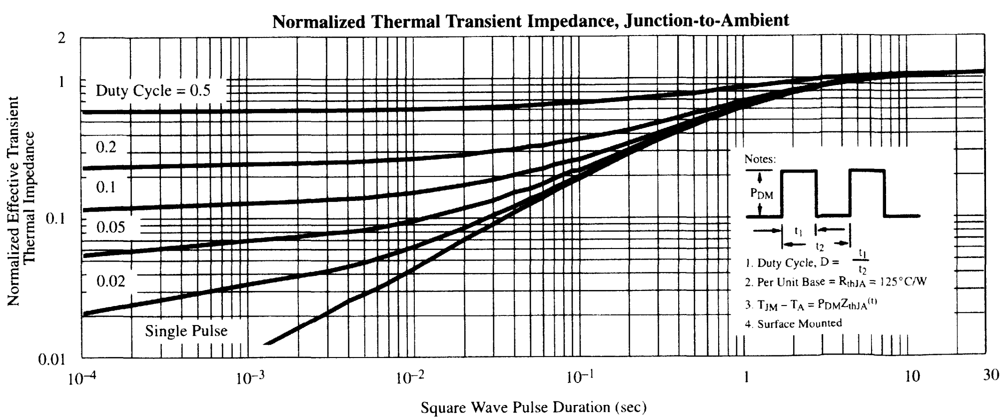
Typical Characteristics (25°C Unless Otherwise Noted)









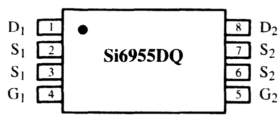


Dual P-Channel Enhancement-Mode MOSFET

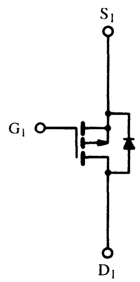
Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
–30	0.085 @ V_{GS} = –10 V	± 2.5
	0.19 @ V_{GS} = –4.5 V	± 1.8

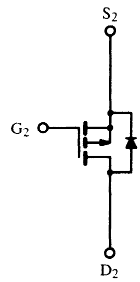
TSSOP-8



Top View



P-Channel MOSFET



P-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	–30	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	± 2.5	A
	T_A = 70°C		± 2.1	
Pulsed Drain Current		I_{DM}	± 20	
Continuous Source Current (Diode Conduction)[a]		I_S	–1.25	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	1.0	W
	T_A = 70°C		0.64	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient[a]	R_{thJA}	125	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70180. A SPICE Model data sheet is available for this product (FaxBack document #70550).

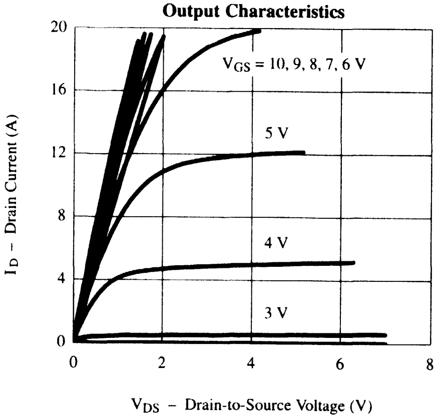
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250\ \mu A$	1.0			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = \pm 20$ V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -30$ V, $V_{GS} = 0$ V			−1	µA
		$V_{DS} = -30$ V, $V_{GS} = 0$ V, $T_J = 55°C$			−25	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \geq -5$ V, $V_{GS} = -10$ V	−15			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	$V_{GS} = -10$ V, $I_D = 2.5$ A		0.066	0.085	Ω
		$V_{GS} = -4.5$ V, $I_D = 1.8$ A		0.125	0.19	
Forward Transconductance[a]	g_{fs}	$V_{DS} = -15$ V, $I_D = -2.5$ A		5		S
Diode Forward Voltage[a]	V_{SD}	$I_S = -1.25$ A, $V_{GS} = 0$ V		0.8	−1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	$V_{DS} = -10$ V, $V_{GS} = -10$ V, $I_D = -2.5$ A		8.7	15	nC
Gate-Source Charge	Q_{gs}			1.9		
Gate-Drain Charge	Q_{gd}			1.3		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10$ V, $R_L = 10\ \Omega$, $I_D \cong -1$ A, $V_{GEN} = -10$ V, $R_G = 6\ \Omega$		7	15	ns
Rise Time	t_r			9	18	
Turn-Off Delay Time	$t_{d(off)}$			14	27	
Fall Time	t_f			8	15	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -1.25$ A, di/dt = 100 A/µs		46	80	

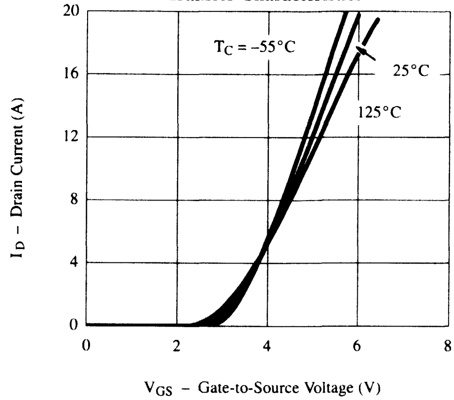
Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

Typical Characteristics (25 °C Unless Otherwise Noted)

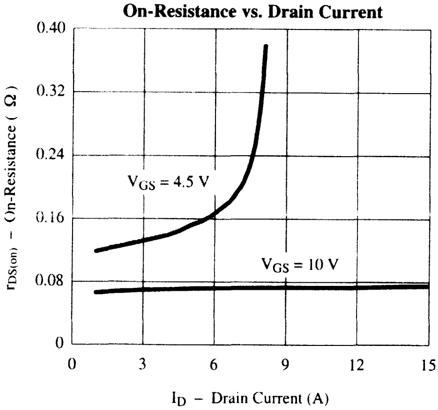
Output Characteristics



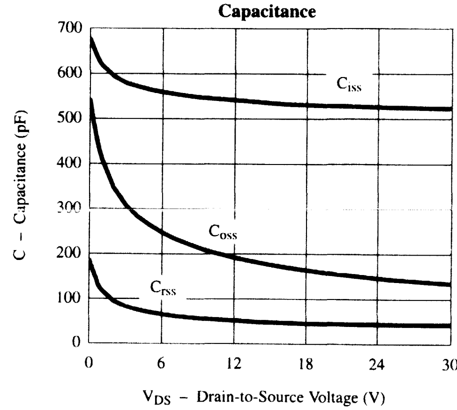
Transfer Characteristics



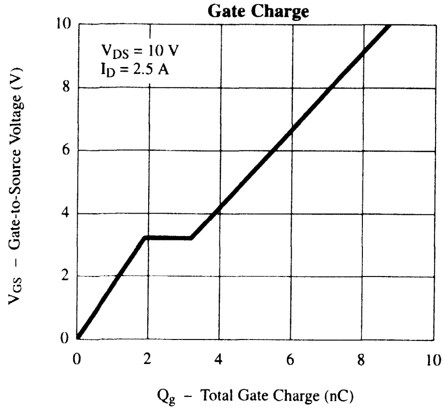
On-Resistance vs. Drain Current



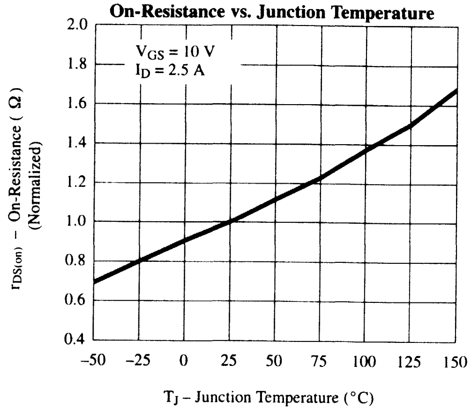
Capacitance



Gate Charge

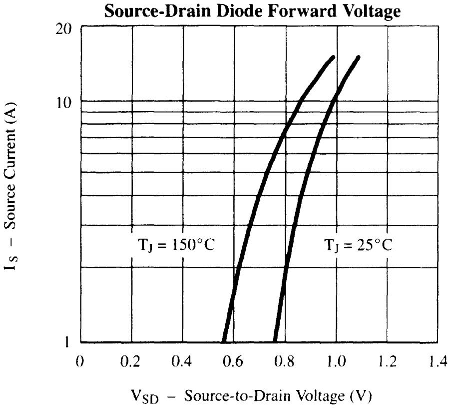


On-Resistance vs. Junction Temperature

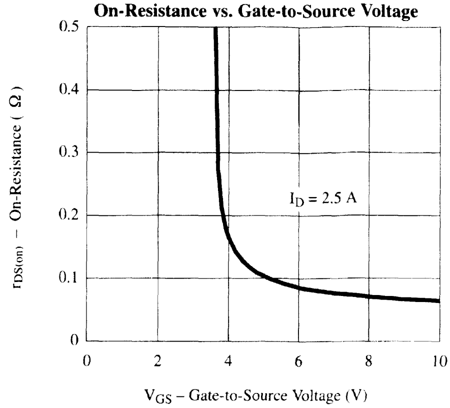


Typical Characteristics (25 °C Unless Otherwise Noted)

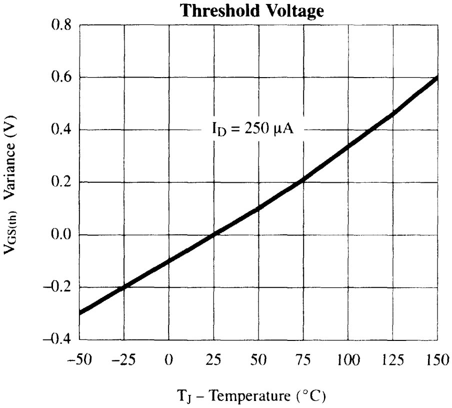
Source-Drain Diode Forward Voltage



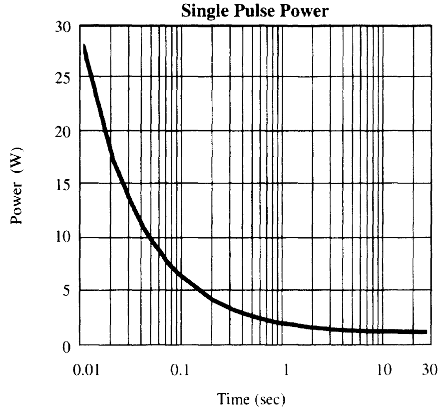
On-Resistance vs. Gate-to-Source Voltage



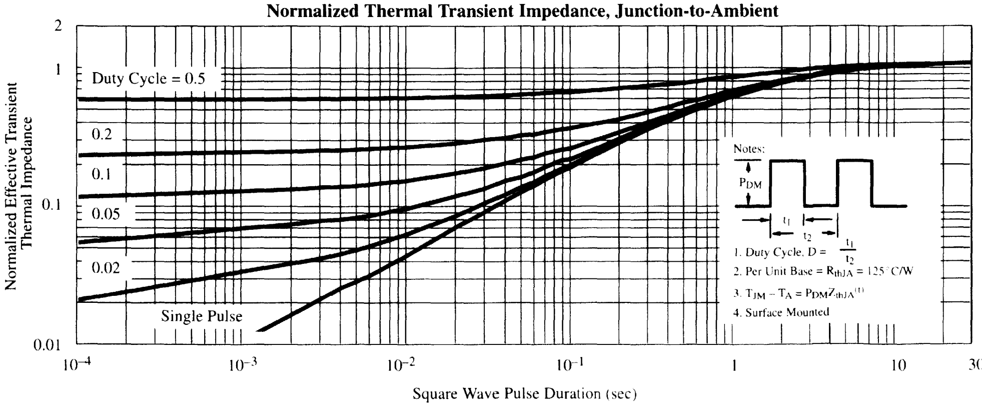
Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient



Triple N-Channel 30-V (D-S) Rated MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
30	0.028 @ V_{GS} = 10 V	±5.6
	0.042 @ V_{GS} = 4.5 V	±4.5

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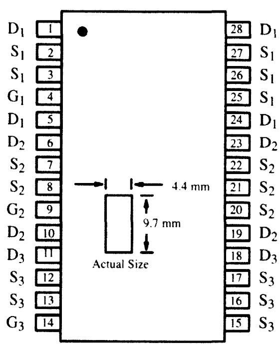
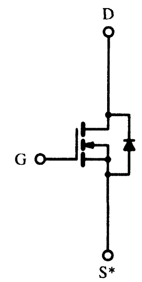


Top View



N-Channel MOSFET

*Source Pins 2, 3, 25, 26, and 27 must be tied common.

Source Pins 7, 8, 20, 21, and 22 must be tied common.

Source Pins 12, 13, 15, 16, and 17 must be tied common.

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	±5.6	A
	T_A = 70°C		±4.4	
Pulsed Drain Current		I_{DM}	±30	
Continuous Source Current (Diode Conduction)[a]		I_S	1.25	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	1.5	W
	T_A = 70°C		1.0	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient[a]	R_{thJA}	83	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 10 sec.

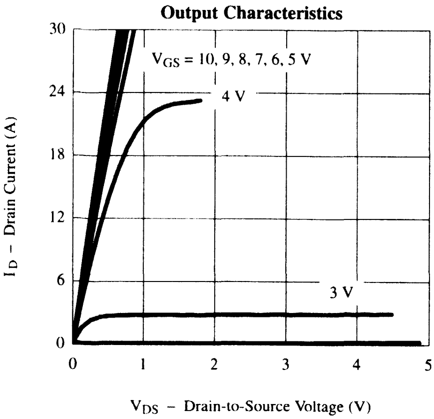
Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70183. A SPICE Model data sheet is available for this product (FaxBack document #70563).

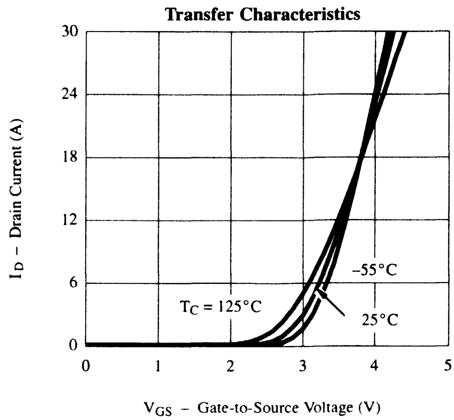
Specifications (T_J = 25°C Unless Otherwise Noted)

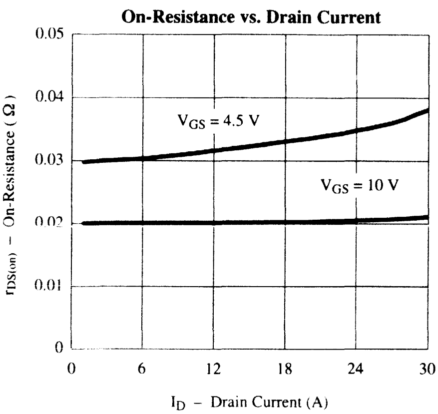
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 µA	1			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V			1	µA
		V_{DS} = 30 V, V_{GS} = 0 V, T_J = 55°C			25	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 10 V	20			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 5.6 A		0.020	0.028	Ω
		V_{GS} = 4.5 V, I_D = 3.5 A		0.030	0.042	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 5.6 A		14		S
Diode Forward Voltage[a]	V_{SD}	I_S = 1.25 A, V_{GS} = 0 V		0.76	1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = 15 V, V_{GS} = 10 V, I_D = 5.6 A		22	30	nC
Gate-Source Charge	Q_{gs}			4.8		
Gate-Drain Charge	Q_{gd}			3.8		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 15 V, R_L = 15 Ω I_D ≅ 1 A, V_{GEN} = 10 V, R_G = 6 Ω		13	20	ns
Rise Time	t_r			10	20	
Turn-Off Delay Time	$t_{d(off)}$			38	55	
Fall Time	t_f			15	30	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 1.25 A, di/dt = 100 A/µs		50	80	

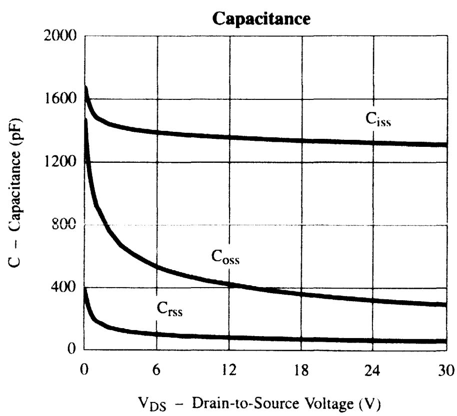
Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

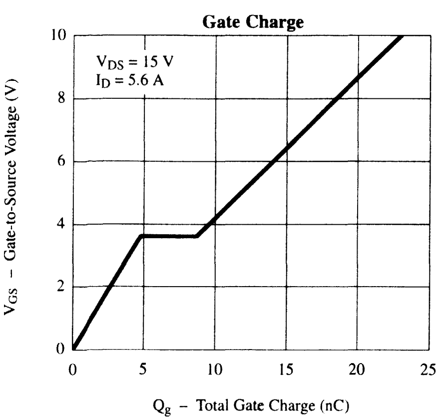
Typical Characteristics (25° C Unless Noted)

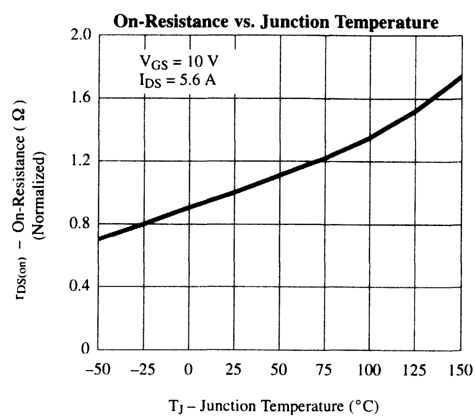






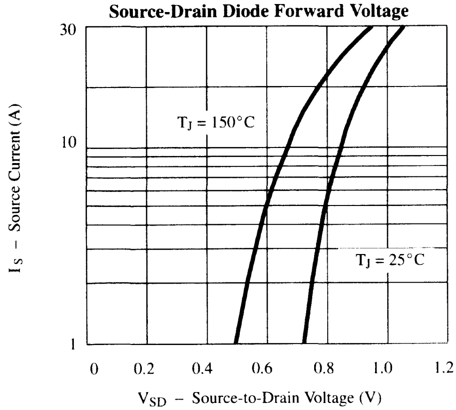




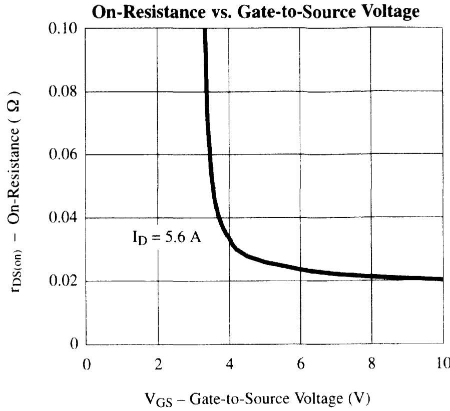


Typical Characteristics (25°C Unless Noted)

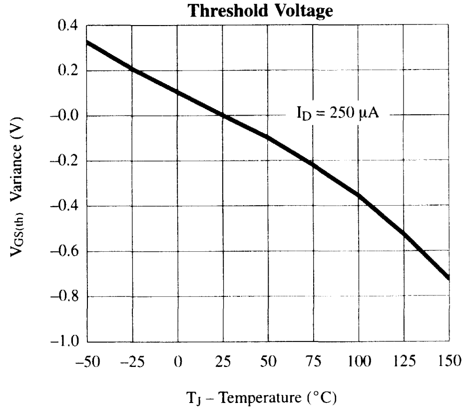
Source-Drain Diode Forward Voltage



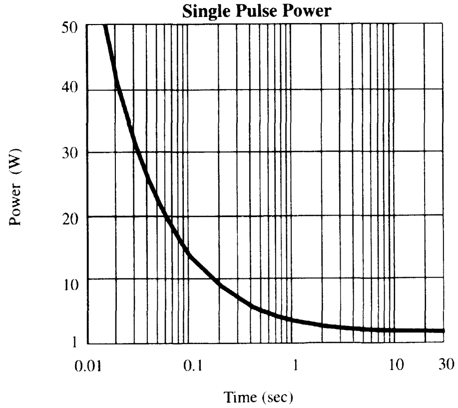
On-Resistance vs. Gate-to-Source Voltage



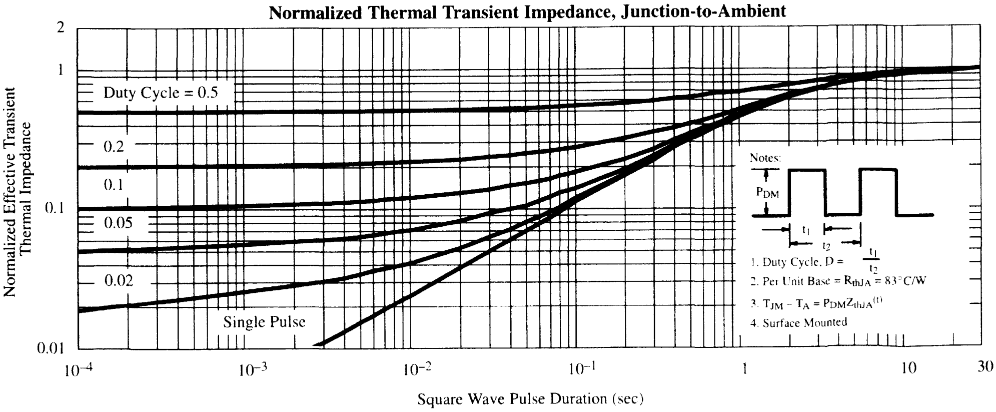
Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient



New Product

Triple P-Channel 30-V (D-S) Rated MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
–30	0.040 @ V_{GS} = –10 V	± 4.5
	0.070 @ V_{GS} = –4.5 V	± 3.4

TrenchFET™ Power MOSFETs

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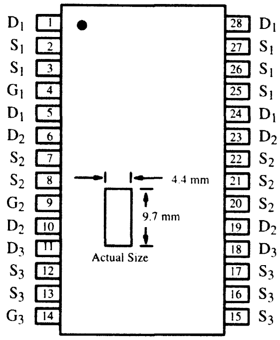
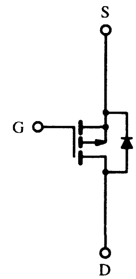


Top View



P-Channel MOSFET

*Source Pins 2, 3, 25, 26, and 27 must be tied common.

Source Pins 7, 8, 20, 21, and 22 must be tied common.

Source Pins 12, 13, 15, 16, and 17 must be tied common.

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	–30	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	± 4.5	A
	T_A = 70°C		± 3.6	
Pulsed Drain Current		I_{DM}	± 30	
Continuous Source Current (Diode Conduction)[a]		I_S	–1.25	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	1.5	W
	T_A = 70°C		1.0	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient[a]	R_{thJA}	83	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70184. A SPICE Model data sheet is available for this product (FaxBack document #70564).

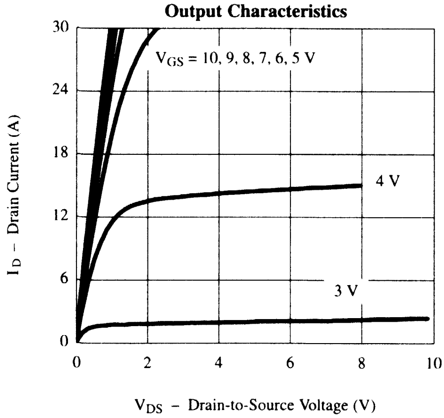
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250\ \mu A$	−1			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = −30 V, V_{GS} = 0 V			−1	µA
		V_{DS} = −30 V, V_{GS} = 0 V, T_J = 55°C			−25	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} = −5 V, V_{GS} = −10 V	−20			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = −10 V, I_D = −4.5 A		0.029	0.040	Ω
		V_{GS} = −4.5 V, I_D = −3.5 A		0.045	0.070	
Forward Transconductance[a]	g_{fs}	V_{DS} = −15 V, I_D = −4.5 A		9.0		S
Diode Forward Voltage[a]	V_{SD}	I_S = −1.25 A, V_{GS} = 0 V		−0.8	−1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = −15 V, V_{GS} = −10 V, I_D = −4.5 A		20	35	nC
Gate-Source Charge	Q_{gs}			4.0		
Gate-Drain Charge	Q_{gd}			3.3		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = −15 V, R_L = 15 Ω $I_D \cong$ −1 A, V_{GEN} = −10 V, R_G = 6 Ω		15	25	ns
Rise Time	t_r			14	25	
Turn-Off Delay Time	$t_{d(off)}$			40	65	
Fall Time	t_f			15	25	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = −1.25 A, di/dt = 100 A/µs		50	80	

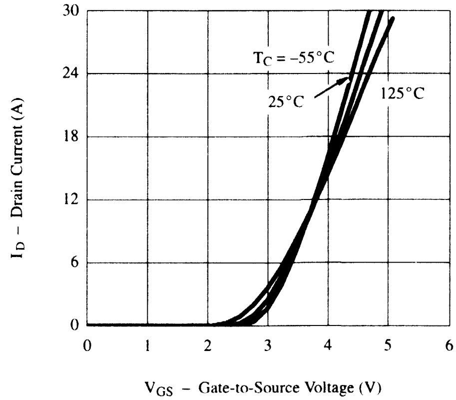
Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

Typical Characteristics (25°C Unless Noted)

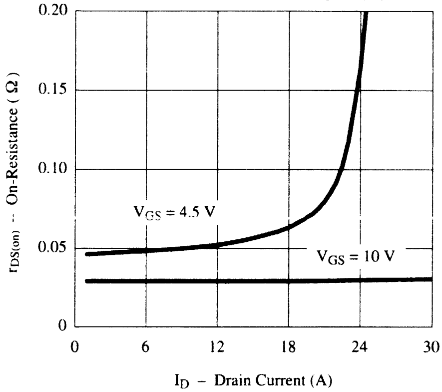
Output Characteristics



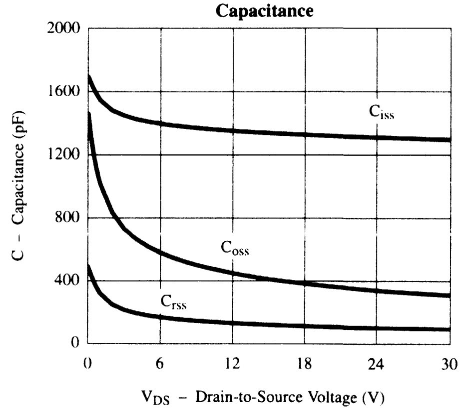
Transfer Characteristics



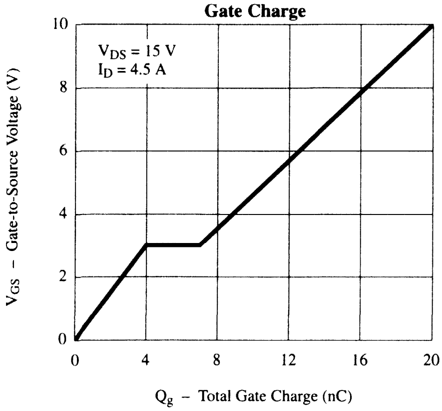
On-Resistance vs. Drain Current



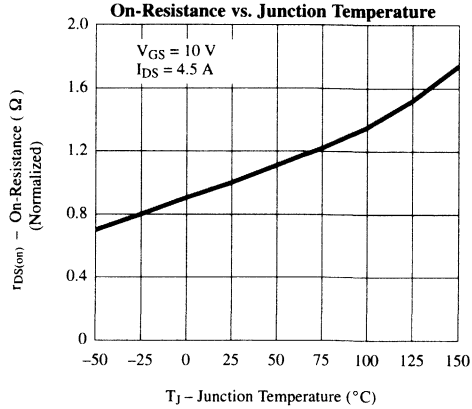
Capacitance



Gate Charge

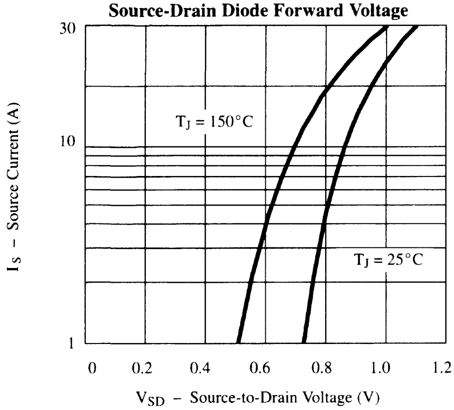


On-Resistance vs. Junction Temperature

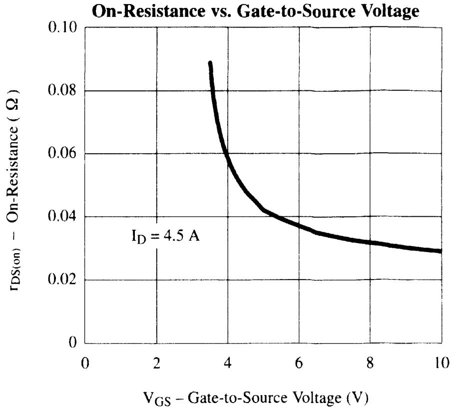


Typical Characteristics (25°C Unless Noted)

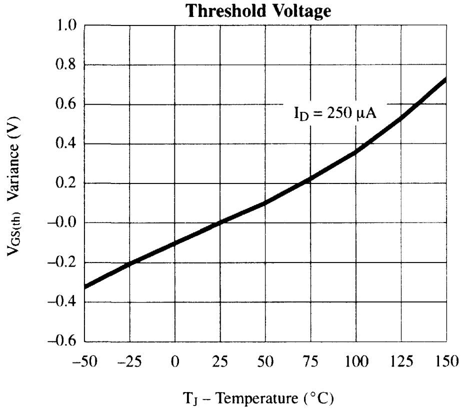
Source-Drain Diode Forward Voltage



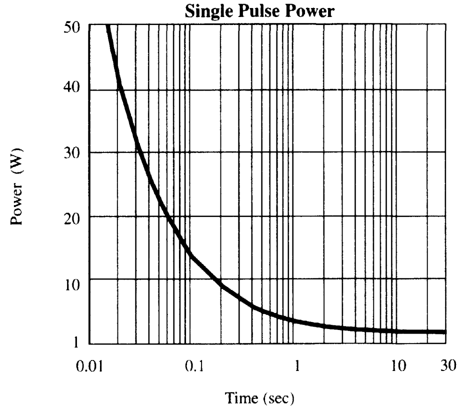
On-Resistance vs. Gate-to-Source Voltage



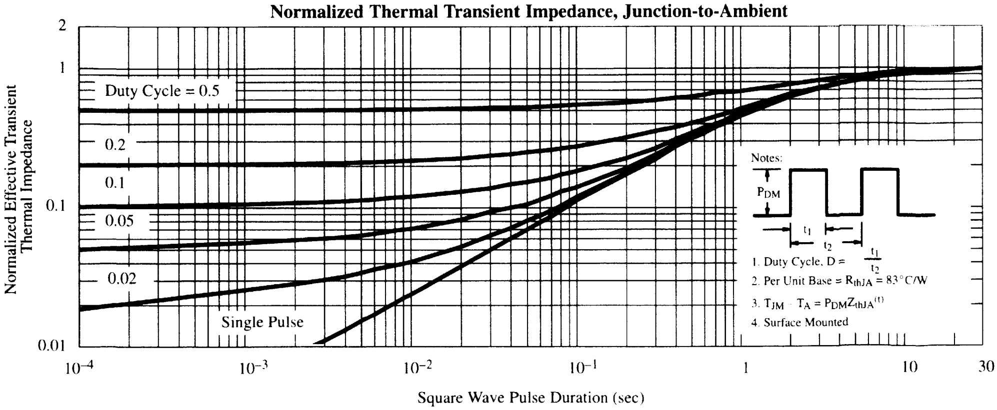
Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient



Triple Complementary 30-V (D-S) Rated Half-Bridge

Product Summary

	V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
N-Channel	30	0.065 @ V_{GS} = 10 V	± 3.6
		0.095 @ V_{GS} = 4.5 V	± 3.0
P-Channel	–30	0.085 @ V_{GS} = –10 V	± 3.1
		0.19 @ V_{GS} = –4.5 V	± 2.1

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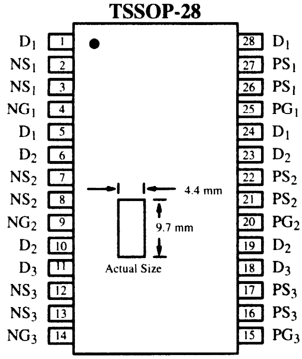
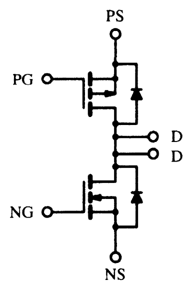


Top View

P-Channel MOSFET



N-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage		V_{DS}	30	–30	V
Gate-Source Voltage		V_{GS}	± 20	± 20	
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	± 3.6	± 3.1	A
	T_A = 70°C		± 2.9	± 2.5	
Pulsed Drain Current		I_{DM}	± 20	± 20	
Continuous Source Current (Diode Conduction)[a]		I_S	1.25	–1.25	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	1.5		W
	T_A = 70°C		1.0		
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150		°C

Thermal Resistance Ratings

Parameter	Symbol	N- or P-Channel	Unit
Maximum Junction-to-Ambient[a]	R_{thJA}	83	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70185.

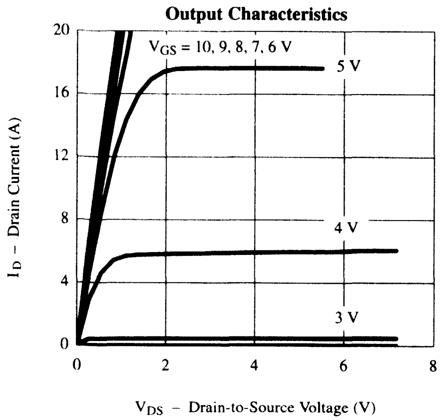
New Product

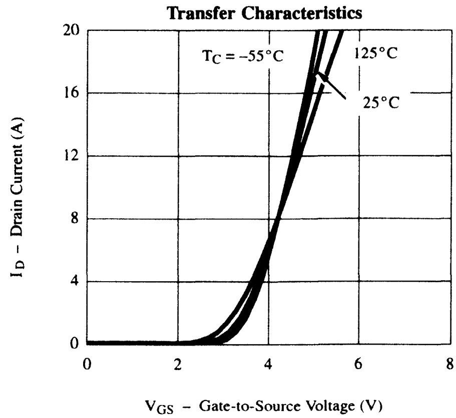
Specifications (T_J = 25°C Unless Otherwise Noted)

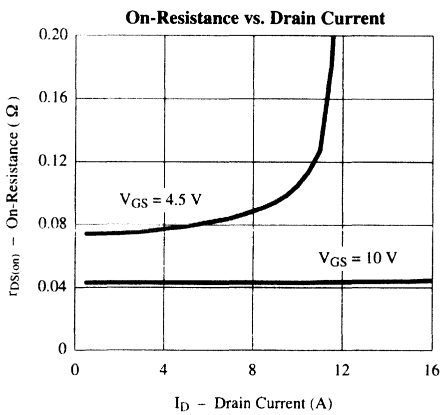
Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Static							
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\ \mu A$	N-Ch	1.0			V
		$V_{DS} = V_{GS}$, $I_D = -250\ \mu A$	P-Ch	−1.0			
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = \pm 20$ V				±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30$ V, $V_{GS} = 0$ V	N-Ch			1	µA
		$V_{DS} = -30$ V, $V_{GS} = 0$ V	P-Ch			−1	
		$V_{DS} = 30$ V, $V_{GS} = 0$ V, $T_J = 55°C$	N-Ch			25	
		$V_{DS} = -30$ V, $V_{GS} = 0$ V, $T_J = 55°C$	P-Ch			−25	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \geq 5$ V, $V_{GS} = 10$ V	N-Ch	15			A
		$V_{DS} \geq -5$ V, $V_{GS} = -10$ V	P-Ch	−15			
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	$V_{GS} = 10$ V, $I_D = 3.6$ A	N-Ch		0.041	0.09	Ω
		$V_{GS} = -10$ V, $I_D = 3.1$ A	P-Ch		0.063	0.085	
		$V_{GS} = 4.5$ V, $I_D = 3.0$ A	N-Ch		0.071	0.095	
		$V_{GS} = -4.5$ V, $I_D = 2.1$ A	P-Ch		0.12	0.19	
Forward Transconductance[a]	g_{fs}	$V_{DS} = 15$ V, $I_D = 3.6$ A	N-Ch		7		S
		$V_{DS} = -15$ V, $I_D = -3.1$ A	P-Ch		5		
Diode Forward Voltage[a]	V_{SD}	$I_S = 1.25$ A, $V_{GS} = 0$ V	N-Ch		0.78	1.2	V
		$I_S = -1.25$ A, $V_{GS} = 0$ V	P-Ch		−0.78	−1.2	
Dynamic[b]							
Total Gate Charge	Q_g	N-Channel $V_{DS} = 15$ V, $V_{GS} = 10$ V, $I_D = 3.6$ A P-Channel $V_{DS} = -15$ V, $V_{GS} = -10$ V, $I_D = -3.1$ A	N-Ch		9.5	15	nC
			P-Ch		8.0	15	
Gate-Source Charge	Q_{gs}		N-Ch		2.5		
			P-Ch		2.3		
Gate-Drain Charge	Q_{gd}		N-Ch		1.2		
			P-Ch		1.2		
Turn-On Delay Time	$t_{d(on)}$	N-Channel $V_{DD} = 10$ V, $R_L = 10\ \Omega$ $I_D \cong 1$ A, $V_{GEN} = 10$ V, $R_G = 6\ \Omega$ P-Channel $V_{DD} = -10$ V, $R_L = 10\ \Omega$ $I_D \cong -1$ A, $V_{GEN} = -10$ V, $R_G = 6\ \Omega$	N-Ch		11	20	ns
			P-Ch		12	25	
Rise Time	t_r		N-Ch		10	20	
			P-Ch		12	25	
Turn-Off Delay Time	$t_{d(off)}$		N-Ch		20	35	
			P-Ch		21	35	
Fall Time	t_f		N-Ch		8	15	
			P-Ch		10	20	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 1.25$ A, di/dt = 100 A/µs	N-Ch		45	70	
		$I_F = -1.25$ A, di/dt = 100 A/µs	P-Ch		40	70	

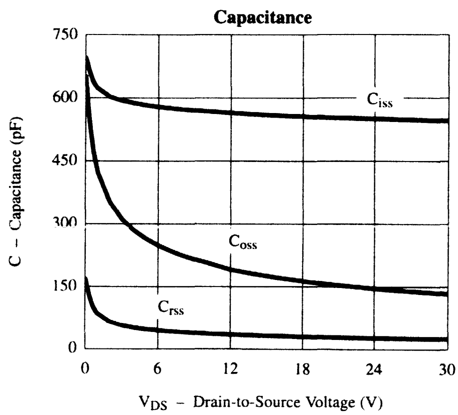
Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

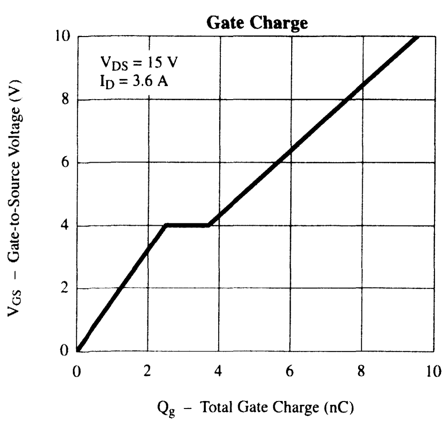
Typical Characteristics (25°C Unless Noted) N-Channel

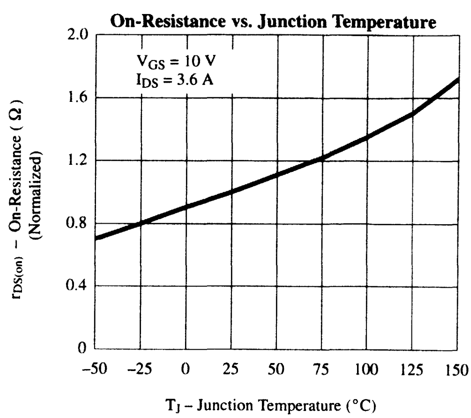






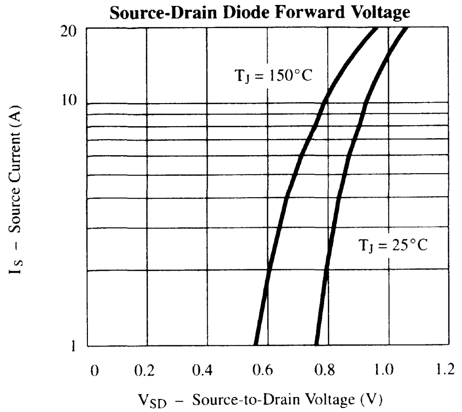


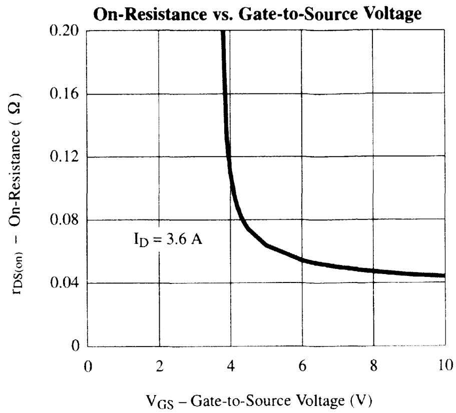


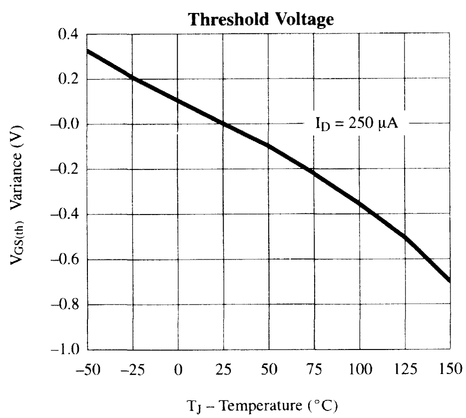


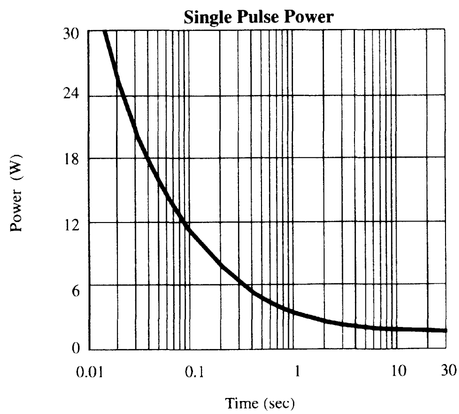
Typical Characteristics (25°C Unless Noted)

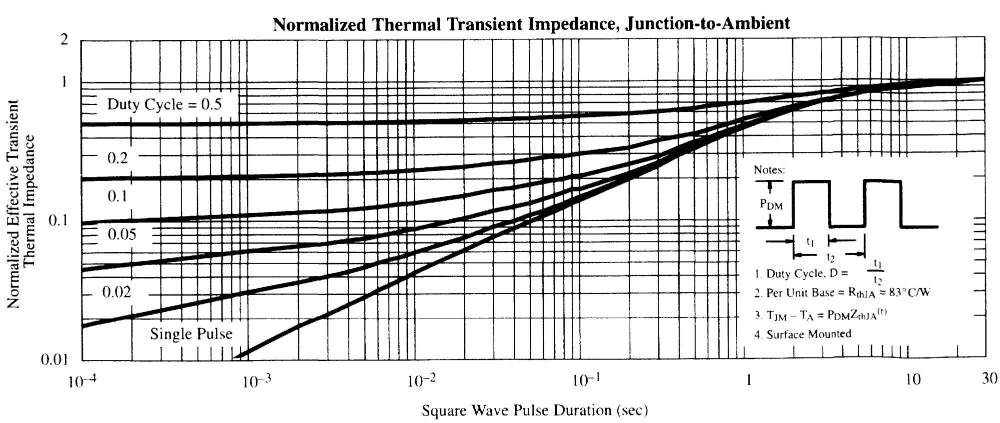
N-Channel







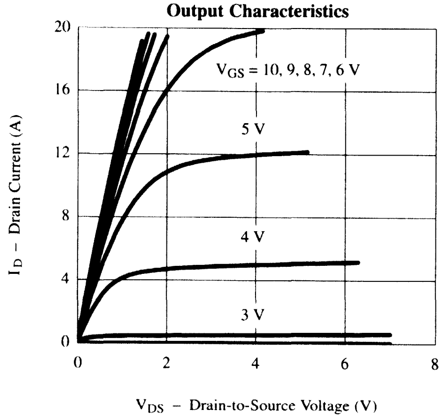




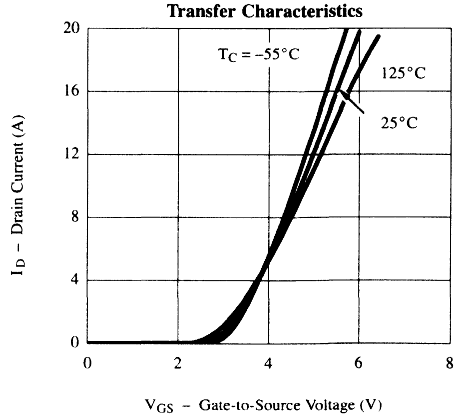
New Product

Typical Characteristics (25°C Unless Noted) — P-Channel

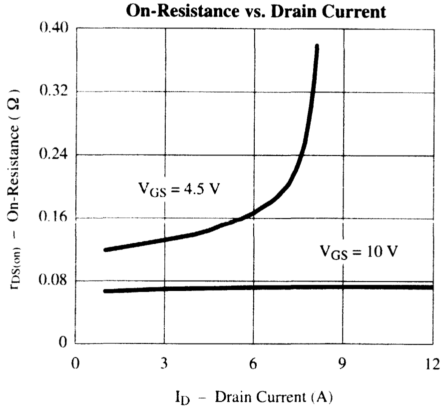
Output Characteristics



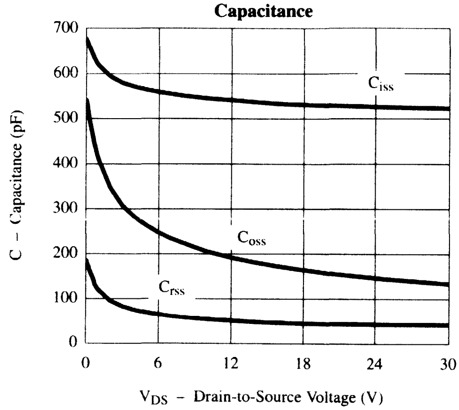
Transfer Characteristics



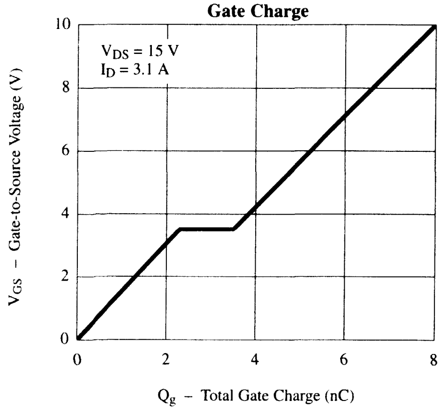
On-Resistance vs. Drain Current



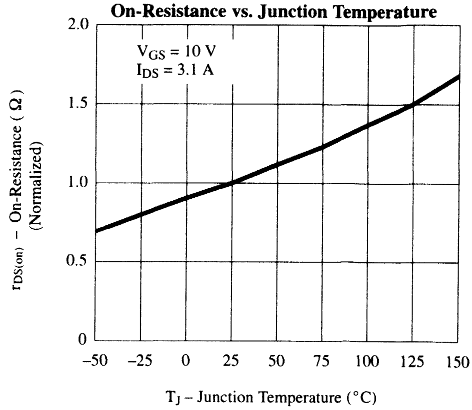
Capacitance



Gate Charge

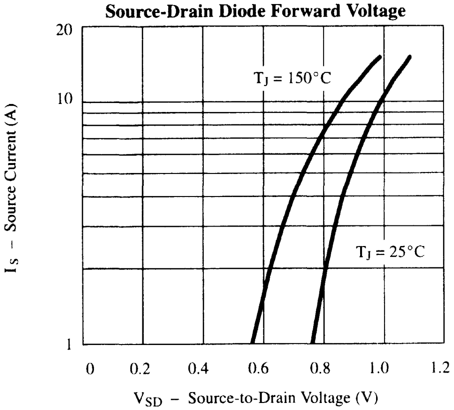


On-Resistance vs. Junction Temperature

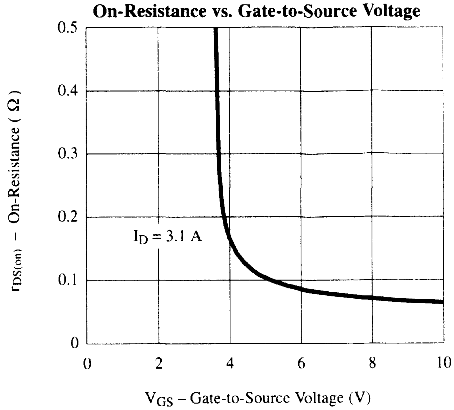


Typical Characteristics (25°C Unless Noted) P-Channel

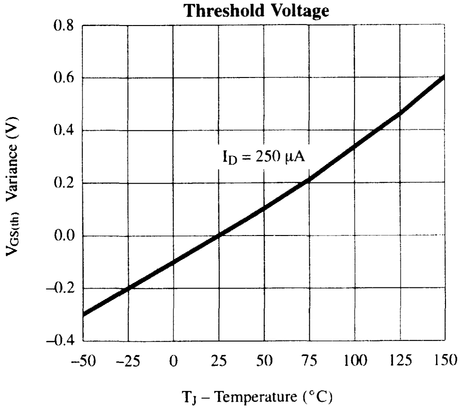
Source-Drain Diode Forward Voltage



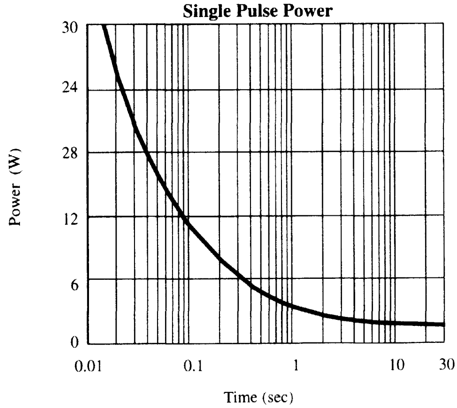
On-Resistance vs. Gate-to-Source Voltage



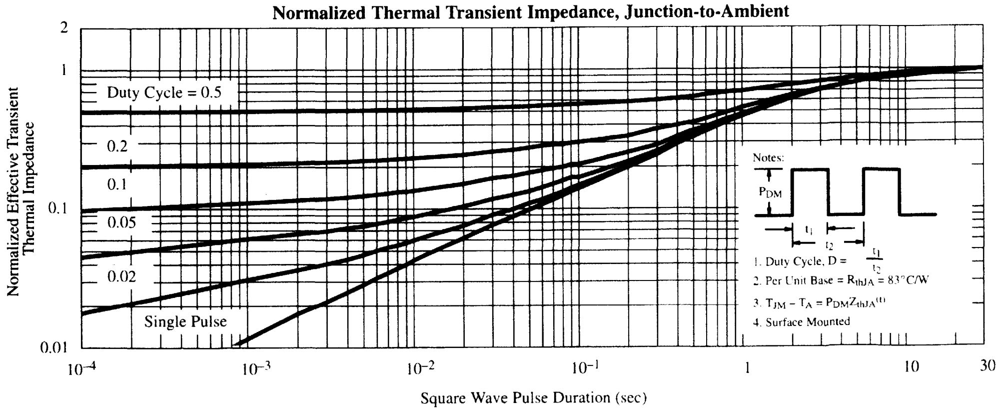
Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient



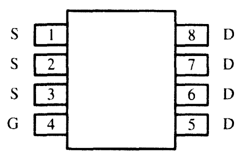
New Product

N-Channel Enhancement-Mode MOSFET

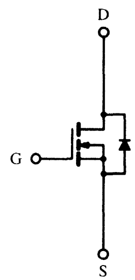
Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
30	0.0135 @ V_{GS} = 10 V	± 10
	0.020 @ V_{GS} = 4.5 V	± 8

SO-8



Top View



N-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	± 10	A
	T_A = 70°C		± 8	
Pulsed Drain Current		I_{DM}	± 50	
Continuous Source Current (Diode Conduction)[a]		I_S	2.3	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	2.5	W
	T_A = 70°C		1.6	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient[a]	R_{thJA}	50	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70148.
A SPICE Model data sheet is available for this product (FaxBack document #70534).

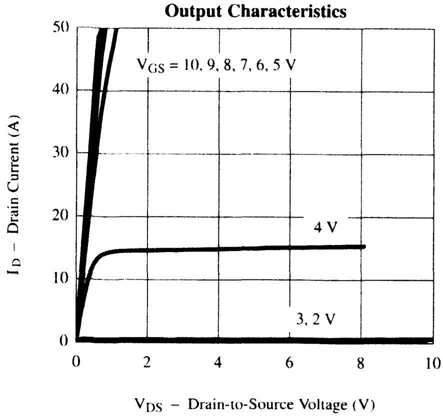
Specifications ($T_J = 25°C$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\ \mu A$	1.0			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = \pm 20$ V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30$ V, $V_{GS} = 0$ V			1	µA
		$V_{DS} = 30$ V, $V_{GS} = 0$ V, $T_J = 55°C$			25	
On-State Drain Current[b]	$I_{D(on)}$	$V_{DS} \geq 5$ V, $V_{GS} = 10$ V	20			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	$V_{GS} = 10$ V, $I_D = 10$ A		0.011	0.0135	Ω
		$V_{GS} = 4.5$ V, $I_D = 5$ A		0.0165	0.020	
Forward Transconductance[b]	g_{fs}	$V_{DS} = 15$ V, $I_D = 10$ A		19		S
Diode Forward Voltage[b]	V_{SD}	$I_S = 2.3$ A, $V_{GS} = 0$ V		0.75	1.1	V
Dynamic[a]						
Total Gate Charge	Q_g	$V_{DS} = 15$ V, $V_{GS} = 10$ V, $I_D = 2$ A		43	60	nC
Gate-Source Charge	Q_{gs}			10		
Gate-Drain Charge	Q_{gd}			7.5		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 25$ V, $R_L = 25\ \Omega$ $I_D \cong 1$ A, $V_{GEN} = 10$ V, $R_G = 6\ \Omega$		17	30	ns
Rise Time	t_r			11	20	
Turn-Off Delay Time	$t_{d(off)}$			60	100	
Fall Time	t_f			45	80	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 2.3$ A, di/dt = 100 A/µs		55	80	

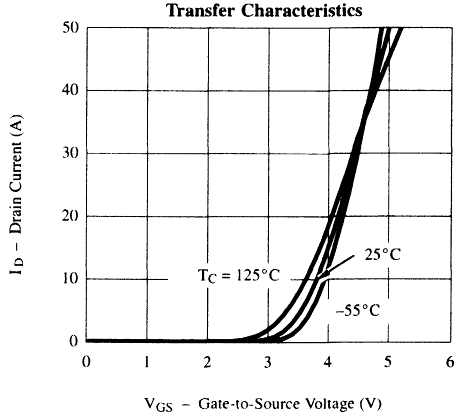
Notes
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

Typical Characteristics (25°C Unless Otherwise Noted)

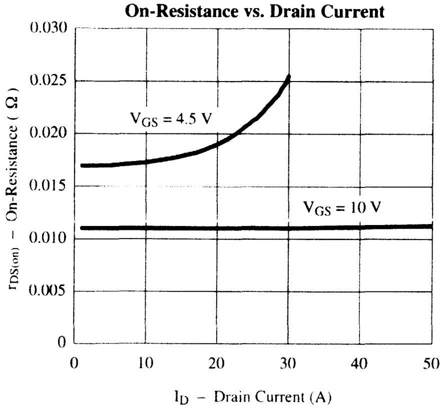
Output Characteristics



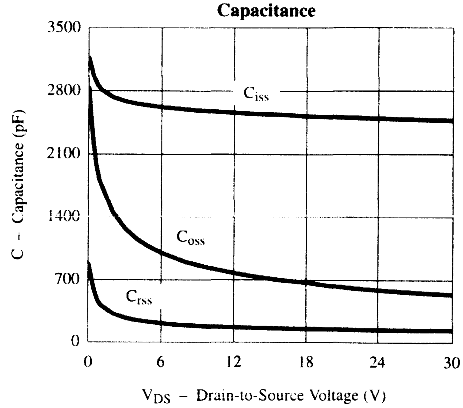
Transfer Characteristics



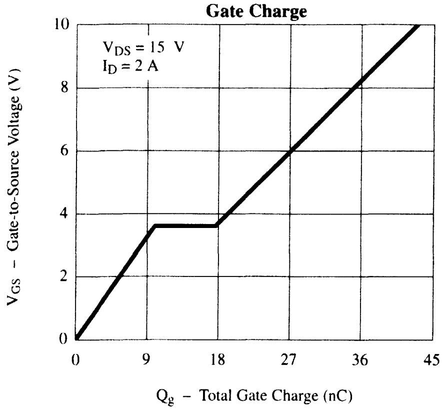
On-Resistance vs. Drain Current



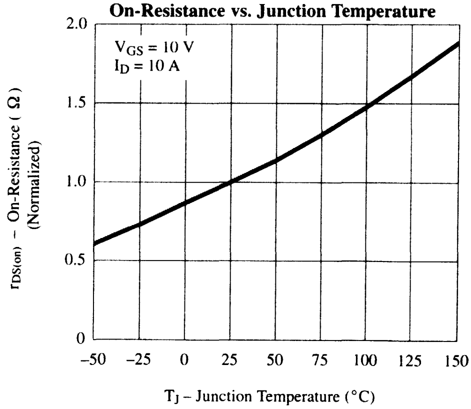
Capacitance



Gate Charge

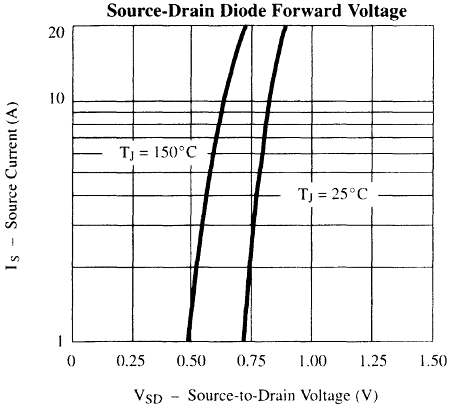


On-Resistance vs. Junction Temperature

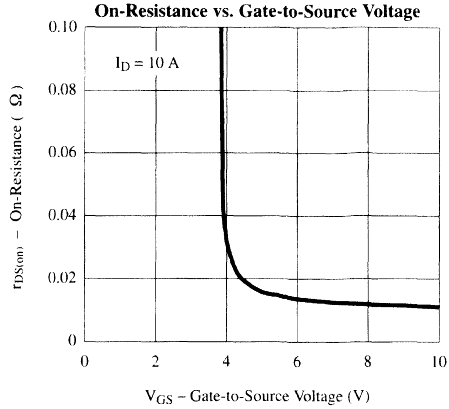


Typical Characteristics (25°C Unless Otherwise Noted)

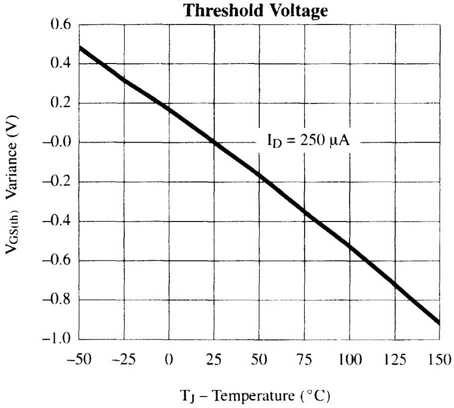
Source-Drain Diode Forward Voltage



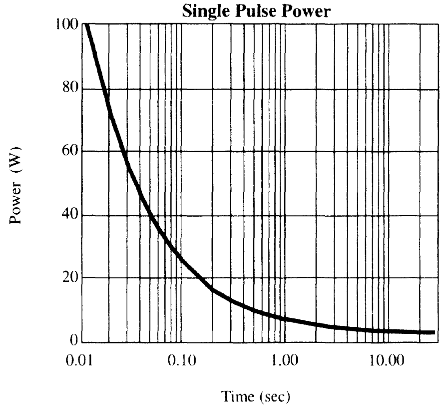
On-Resistance vs. Gate-to-Source Voltage



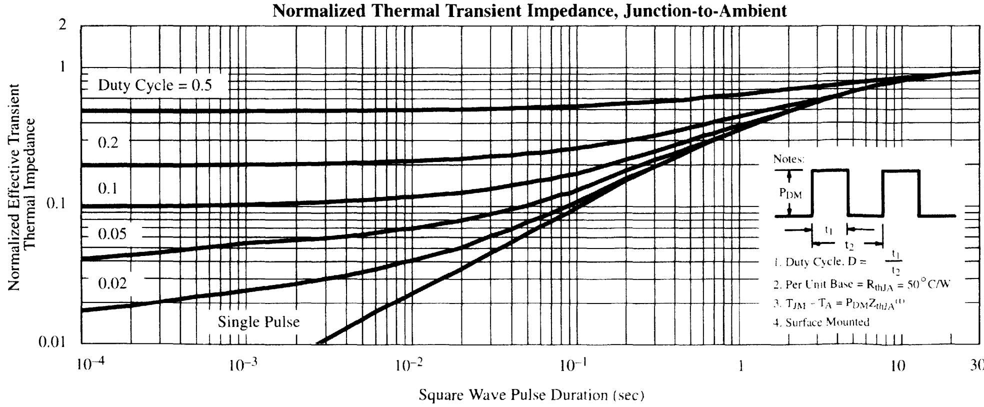
Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient



N-Channel Enhancement-Mode MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
30	0.028 @ V_{GS} = 10 V	± 7.0
	0.042 @ V_{GS} = 4.5 V	± 5.8

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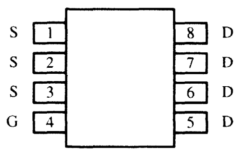
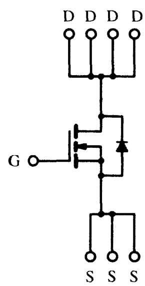


Top View



N-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	± 7.0	A
	T_A = 70°C		± 5.8	
Pulsed Drain Current		I_{DM}	± 30	
Continuous Source Current (Diode Conduction)[a]		I_S	2.3	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	2.5	W
	T_A = 70°C		1.6	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient[a]	R_{thJA}	50	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70154. A SPICE Model data sheet is available for this product (FaxBack document #70552).

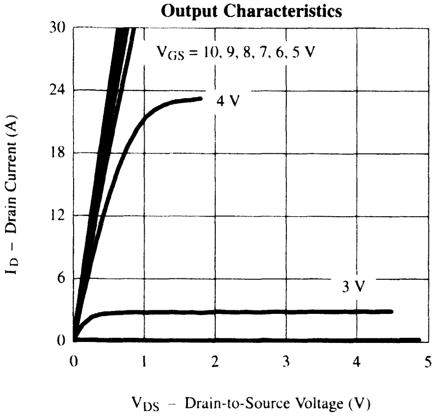
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 µA	1.0			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V			2	µA
		V_{DS} = 30 V, V_{GS} = 0 V, T_J = 55°C			25	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 10 V	30			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D =7.0 A		0.021	0.028	Ω
		V_{GS} = 4.5 V, I_D = 3.5 A		0.030	0.042	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 7.0 A		16		S
Diode Forward Voltage[b]	V_{SD}	I_S = 2 A, V_{GS} = 0 V		0.75	1.1	V
Dynamic[a]						
Total Gate Charge	Q_g	V_{DS} = 15 V, V_{GS} = 10 V, I_D = 2 A		19.5	29	nC
Gate-Source Charge	Q_{gs}			3.4		
Gate-Drain Charge	Q_{gd}			2.7		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 25 V, R_L = 25 Ω I_D ≅ 1 A, V_{GEN} = 10 V, R_G = 6 Ω		9	15	ns
Rise Time	t_r			12	20	
Turn-Off Delay Time	$t_{d(off)}$			38	55	
Fall Time	t_f			19	28	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 2 A, di/dt = 100 A/µs		45	80	

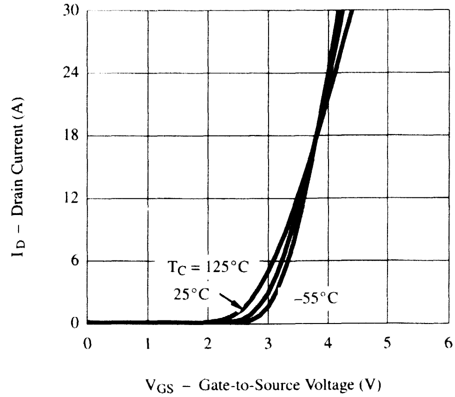
Notes
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

Typical Characteristics (25 °C Unless Otherwise Noted)

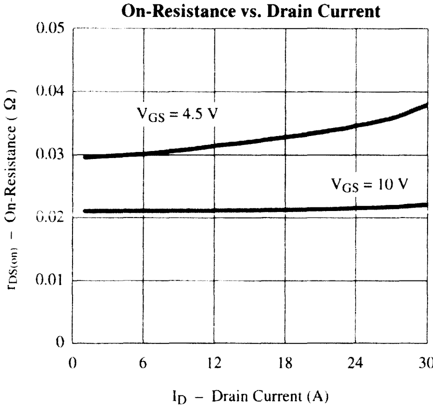
Output Characteristics



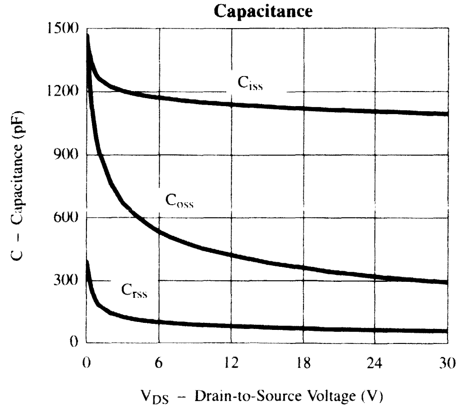
Transfer Characteristics



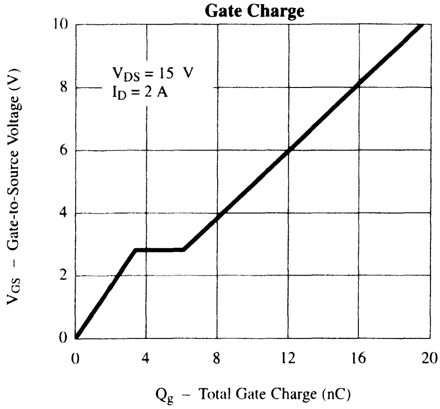
On-Resistance vs. Drain Current



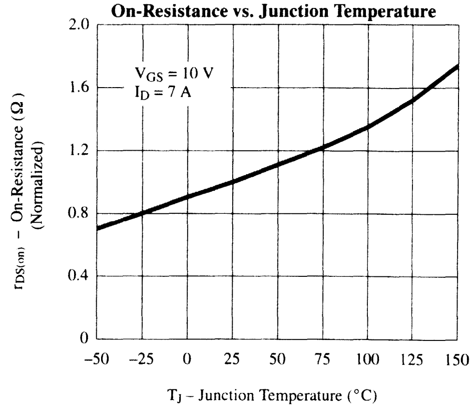
Capacitance



Gate Charge



On-Resistance vs. Junction Temperature



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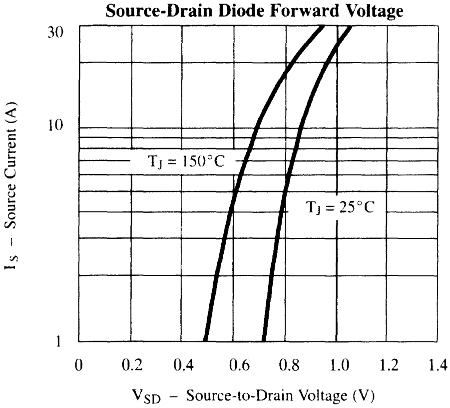
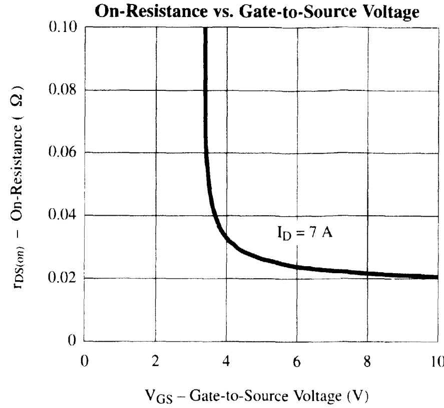
Typical Characteristics (25°C Unless Otherwise Noted)

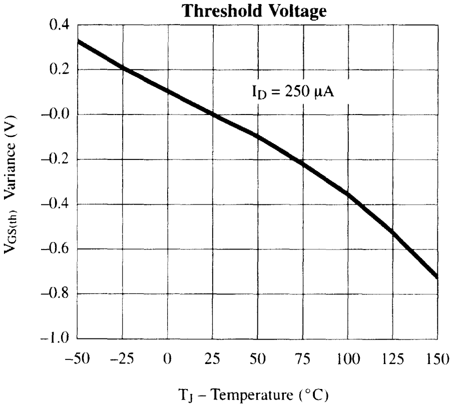
Source-Drain Diode Forward Voltage



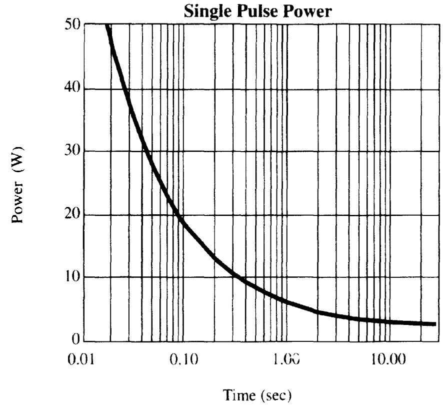
On-Resistance vs. Gate-to-Source Voltage



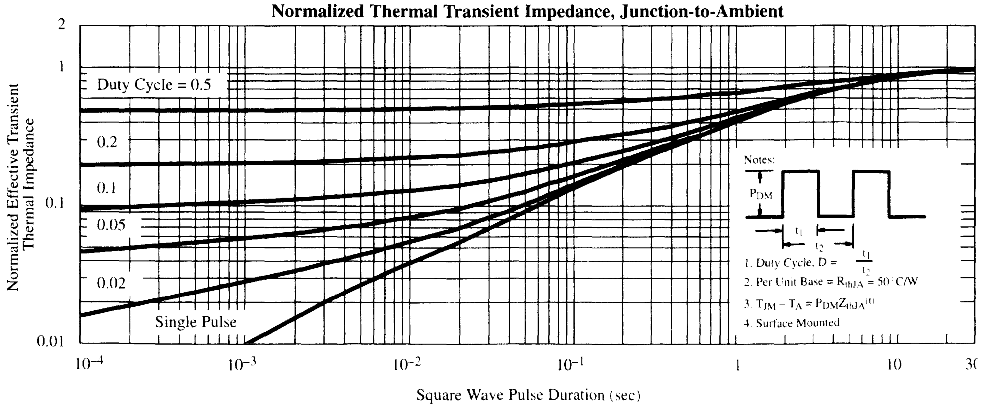
Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient



N-Channel 30-V (D-S) Rated MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
30	0.009 @ V_{GS} = 10 V	± 12.5
	0.013 @ V_{GS} = 4.5 V	± 10.5

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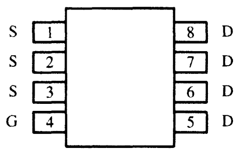
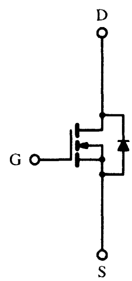


Top View



N-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	± 12.5	A
	T_A = 70°C		± 10.0	A
Pulsed Drain Current		I_{DM}	± 50	A
Continuous Source Current (Diode Conduction)[a]		I_S	2.3	A
Maximum Power Dissipation[a]	T_A = 25°C	P_D	2.5	W
	T_A = 70°C		1.6	W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient[a]	R_{thJA}	50	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70647.

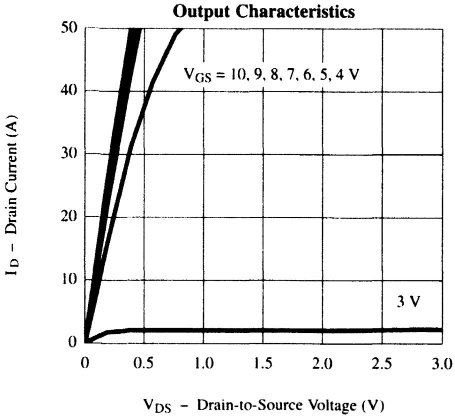
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 µA	1.0			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V			1	µA
		V_{DS} = 30 V, V_{GS} = 0 V, T_J = 55°C			5	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 10 V	30			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D =12.5 A		0.0075	0.009	Ω
		V_{GS} = 4.5 V, I_D = 10.5 A		0.010	0.013	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 12.5 A		50		S
Diode Forward Voltage[b]	V_{SD}	I_S = 2.3 A, V_{GS} = 0 V			1.1	V
Dynamic[a]						
Total Gate Charge	Q_g	V_{DS} = 15 V, V_{GS} = 10 V, I_D = 12.5 A		70	120	nC
Gate-Source Charge	Q_{gs}			18		
Gate-Drain Charge	Q_{gd}			9		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 15 V, R_L = 15 Ω I_D ≅ 1 A, V_{GEN} = 10 V, R_G = 6 Ω		16	25	ns
Rise Time	t_r			15	25	
Turn-Off Delay Time	$t_{d(off)}$			120	200	
Fall Time	t_f			35	70	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 2.3 A, di/dt = 100 A/µs		49	90	

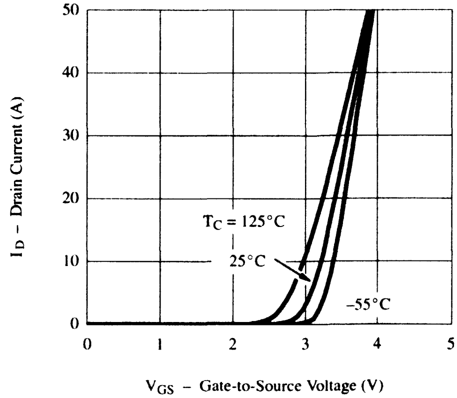
Notes
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

Typical Characteristics (25° C Unless Otherwise Noted)

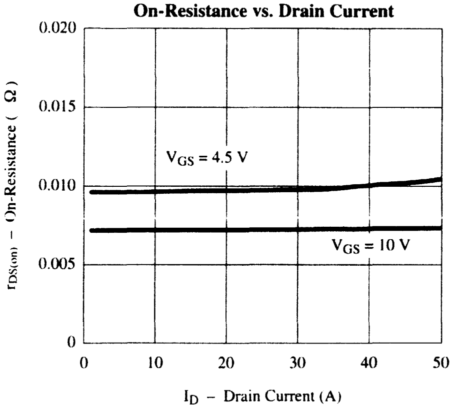
Output Characteristics



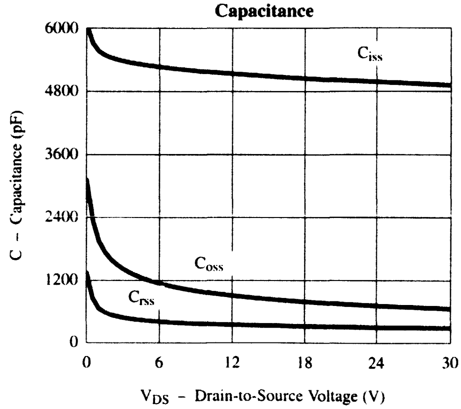
Transfer Characteristics



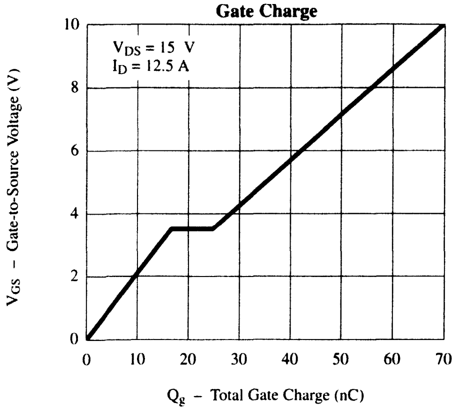
On-Resistance vs. Drain Current



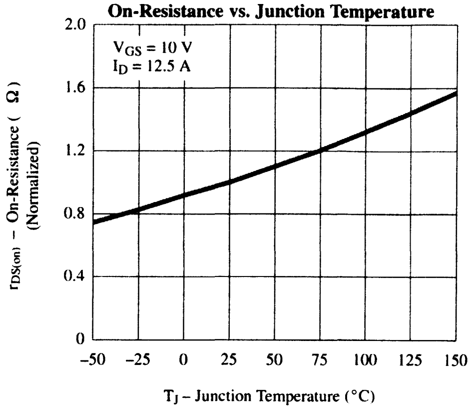
Capacitance



Gate Charge



On-Resistance vs. Junction Temperature



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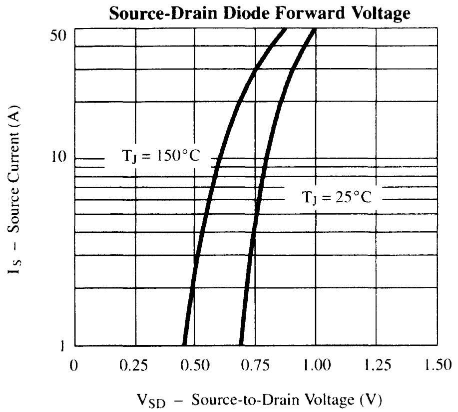
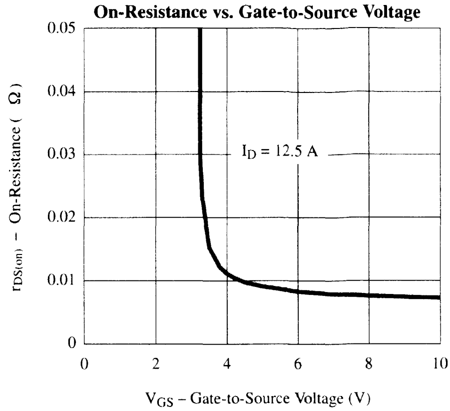
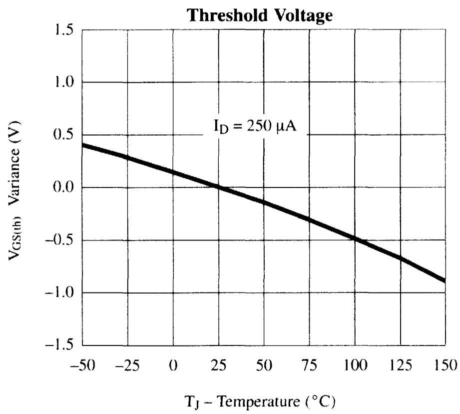
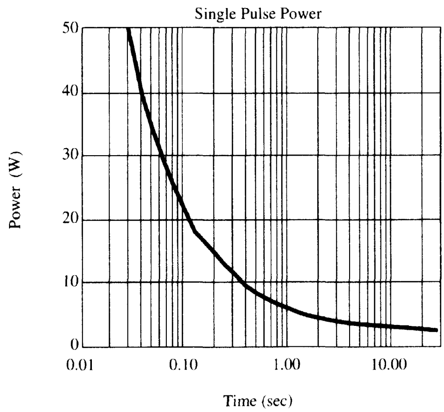
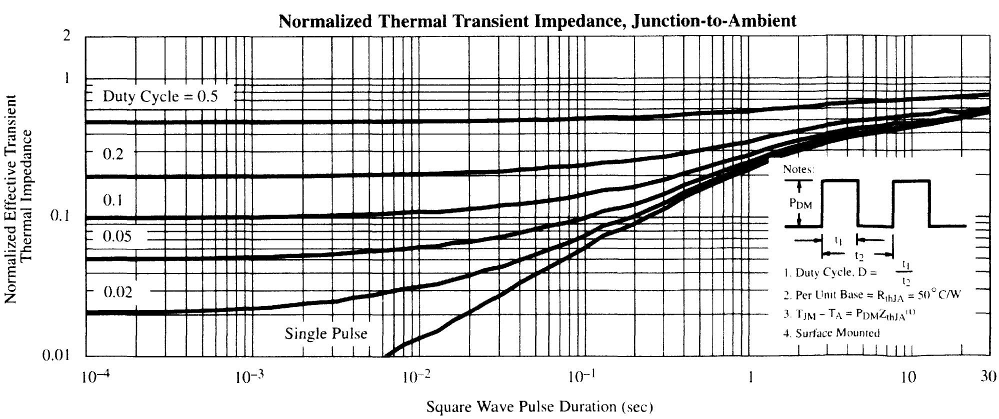
Typical Characteristics (25°C Unless Otherwise Noted)











P-Channel 30-V (D-S) Rated MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
−30	0.014 @ V_{GS} = −10 V	± 11
	0.023 @ V_{GS} = −4.5 V	± 8.5

TrenchFET™ Power MOSFETs

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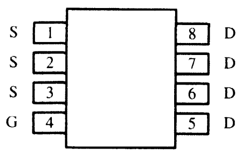
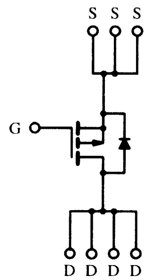


Top View



P-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	−30	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	± 11	A
	T_A = 70°C		± 8.7	
Pulsed Drain Current		I_{DM}	± 50	
Continuous Source Current (Diode Conduction)[a]		I_S	−2.1	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	2.5	W
	T_A = 70°C		1.6	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient[a]	R_{thJA}	50	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70641.

New Product

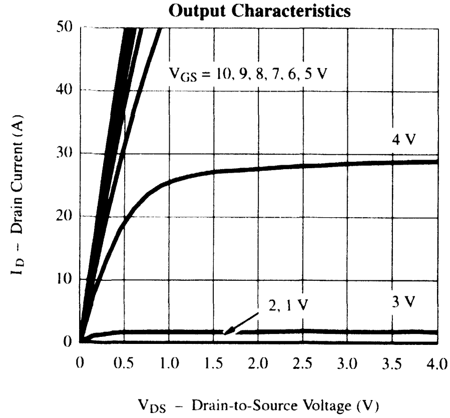
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250\ \mu A$	−1.0			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = \pm 20$ V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -30$ V, $V_{GS} = 0$ V			−1	µA
		$V_{DS} = -15$ V, $V_{GS} = 0$ V, $T_J = 70°C$			−5	
On-State Drain Current[b]	$I_{D(on)}$	$V_{DS} \leq -5$ V, $V_{GS} = -10$ V	30			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	$V_{GS} = -10$ V, $I_D = -11$ A		0.010	0.014	Ω
		$V_{GS} = -4.5$ V, $I_D = -8.5$ A		0.017	0.023	
Forward Transconductance[b]	g_{fs}	$V_{DS} = -15$ V, $I_D = -11$ A		37		S
Diode Forward Voltage[b]	V_{SD}	$I_S = -2.1$ A, $V_{GS} = 0$ V			−1.2	V
Dynamic[a]						
Total Gate Charge	Q_g	$V_{DS} = -15$ V, $V_{GS} = -10$ V, $I_D = -11$ A		74	120	nC
Gate-Source Charge	Q_{gs}			18		
Gate-Drain Charge	Q_{gd}			13		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -15$ V, $R_L = 15\ \Omega$ $I_D \cong -1$ A, $V_{GEN} = -10$ V, $R_G = 6\ \Omega$		16	25	ns
Rise Time	t_r			11	25	
Turn-Off Delay Time	$t_{d(off)}$			122	200	
Fall Time	t_f			40	80	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -2.1$ A, di/dt = 100 A/µs		49	90	

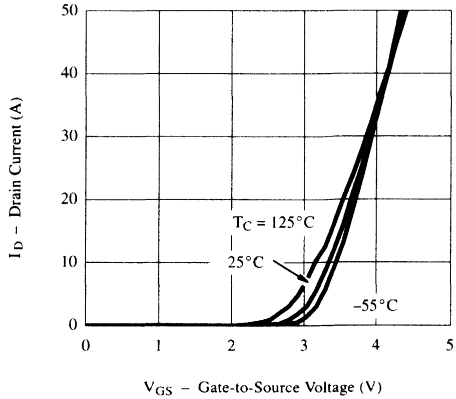
Notes
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

Typical Characteristics (25 °C Unless Otherwise Noted)

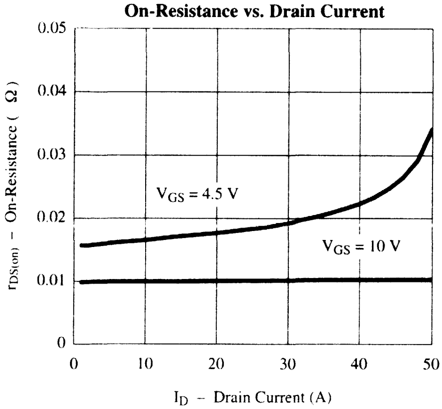
Output Characteristics



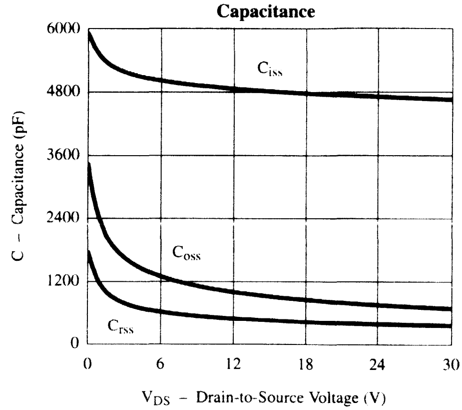
Transfer Characteristics



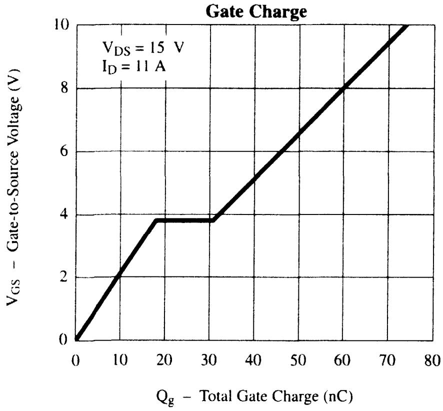
On-Resistance vs. Drain Current



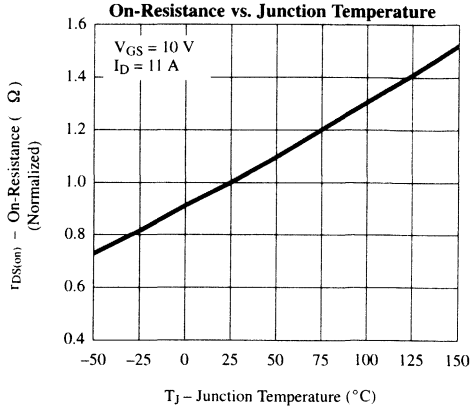
Capacitance



Gate Charge

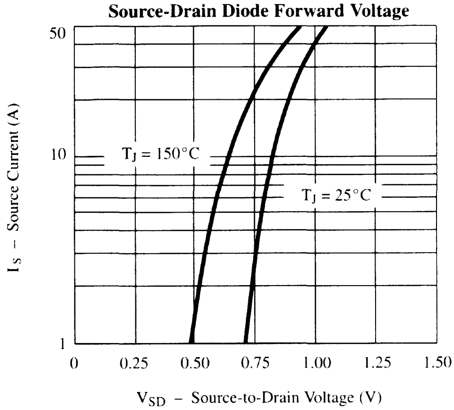


On-Resistance vs. Junction Temperature

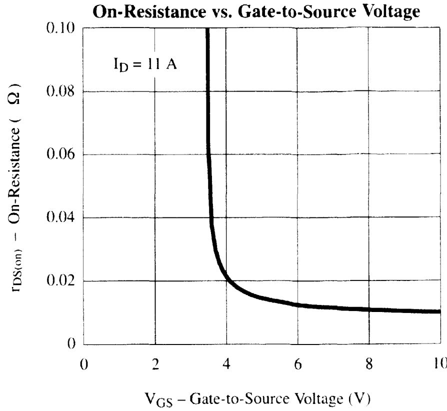


Typical Characteristics (25 °C Unless Otherwise Noted)

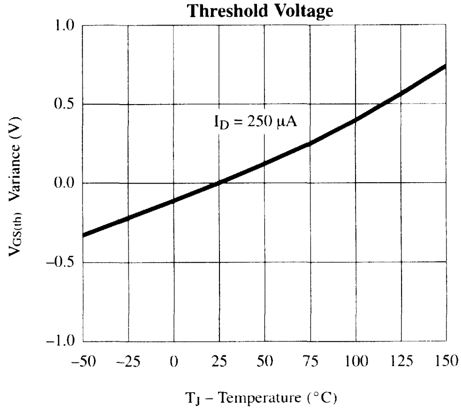
Source-Drain Diode Forward Voltage



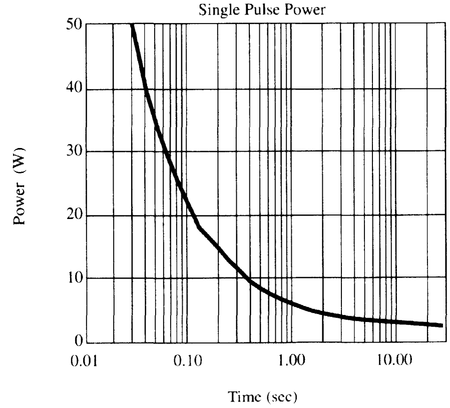
On-Resistance vs. Gate-to-Source Voltage



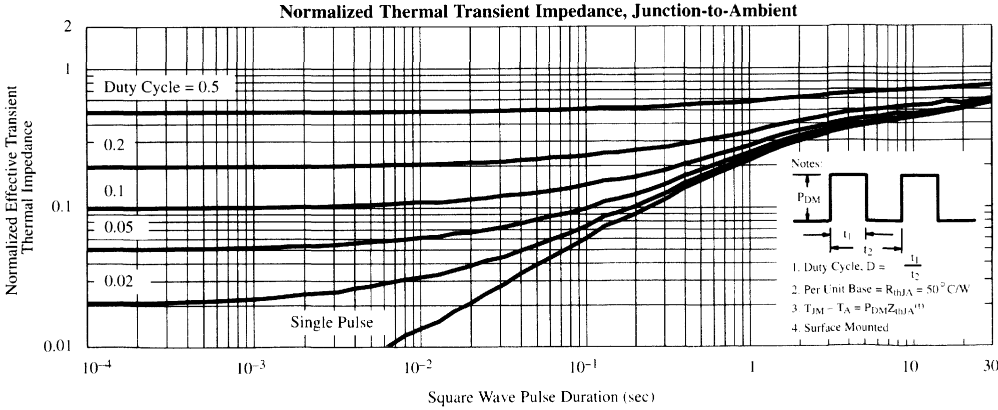
Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient



New Product

P-Channel Enhancement-Mode MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
–30	0.040 @ V_{GS} = –10 V	± 5.8
	0.070 @ V_{GS} = –4.5 V	± 4.5

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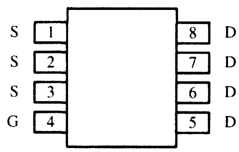
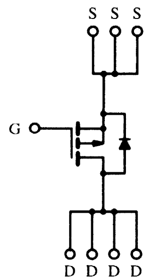


Top View



P-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	–30	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	± 5.8	A
	T_A = 70°C		± 4.6	
Pulsed Drain Current		I_{DM}	± 30	
Continuous Source Current (Diode Conduction)[a]		I_S	–2.3	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	2.5	W
	T_A = 70°C		1.6	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient[a]	R_{thJA}	50	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 10 sec.

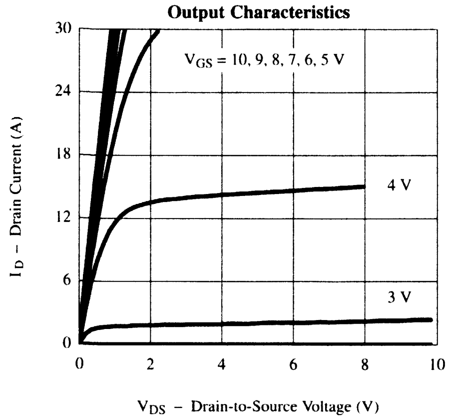
Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70151. A SPICE Model data sheet is available for this product (FaxBack document #70553).

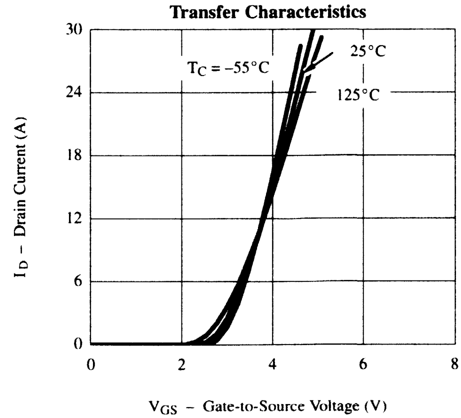
Specifications (T_J = 25°C Unless Otherwise Noted)

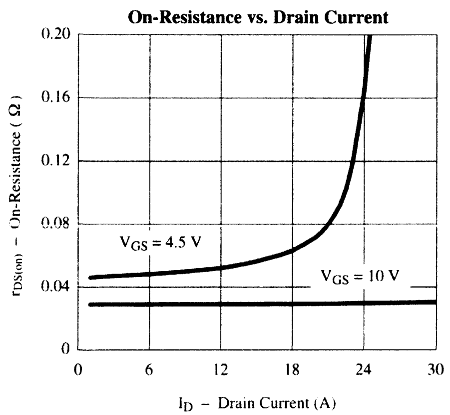
Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250\ \mu A$	–1.0			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = \pm 20$ V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -30$ V, $V_{GS} = 0$ V			–1	µA
		$V_{DS} = -30$ V, $V_{GS} = 0$ V, $T_J = 70°C$			–25	
On-State Drain Current[b]	$I_{D(on)}$	$V_{DS} \leq -5$ V, $V_{GS} = -10$ V	–30			A
		$V_{DS} \leq -5$ V, $V_{GS} = -4.5$ V	–7			
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	$V_{GS} = -10$ V, $I_D = -5.3$ A		0.029	0.040	Ω
		$V_{GS} = -4.5$ V, $I_D = -2.0$ A		0.047	0.070	
Forward Transconductance[b]	g_{fs}	$V_{DS} = -15$ V, $I_D = -5.3$ A		9.3		S
Diode Forward Voltage[b]	V_{SD}	$I_S = -2.3$ A, $V_{GS} = 0$ V		–0.78	–1.2	V
Dynamic[a]						
Total Gate Charge	Q_g	$V_{DS} = -15$ V, $V_{GS} = -10$ V, $I_D = -5.3$ A		22	35	nC
Gate-Source Charge	Q_{gs}			3.95		
Gate-Drain Charge	Q_{gd}			3.5		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -15$ V, $R_L = 15\ \Omega$ $I_D \cong -1$ A, $V_{GEN} = -10$ V, $R_G = 6\ \Omega$		11.5	20	ns
Rise Time	t_r			12	20	
Turn-Off Delay Time	$t_{d(off)}$			38	55	
Fall Time	t_f			15	25	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -2.3$ A, di/dt = 100 A/µs		50	80	

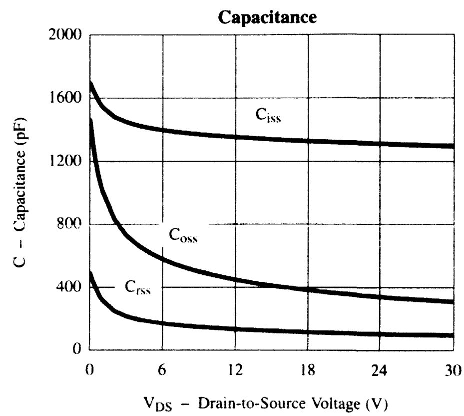
Notes
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

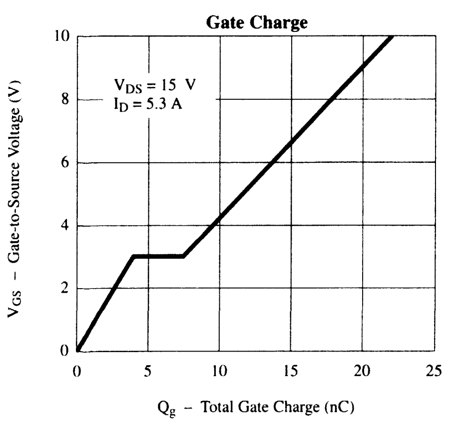
Typical Characteristics (25°C Unless Otherwise Noted)

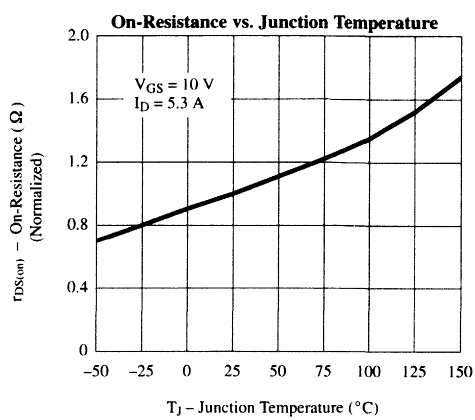












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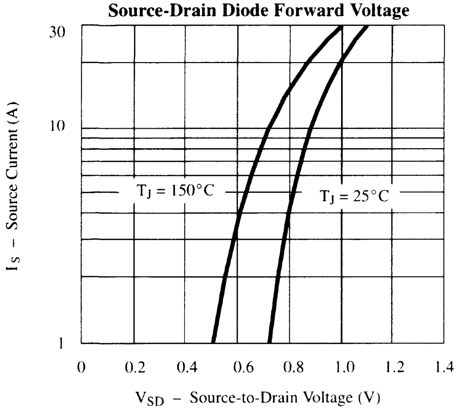
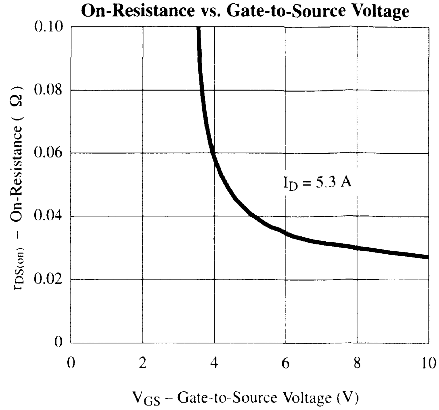
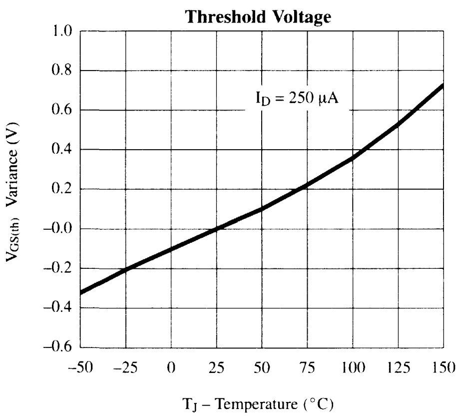
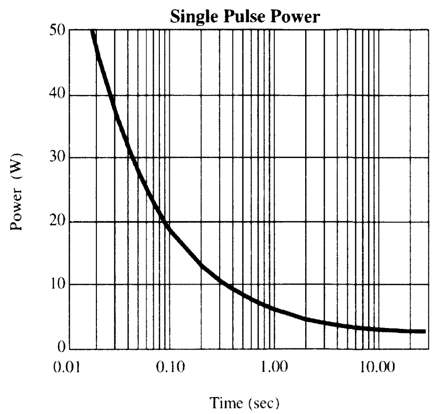
SOIC-8

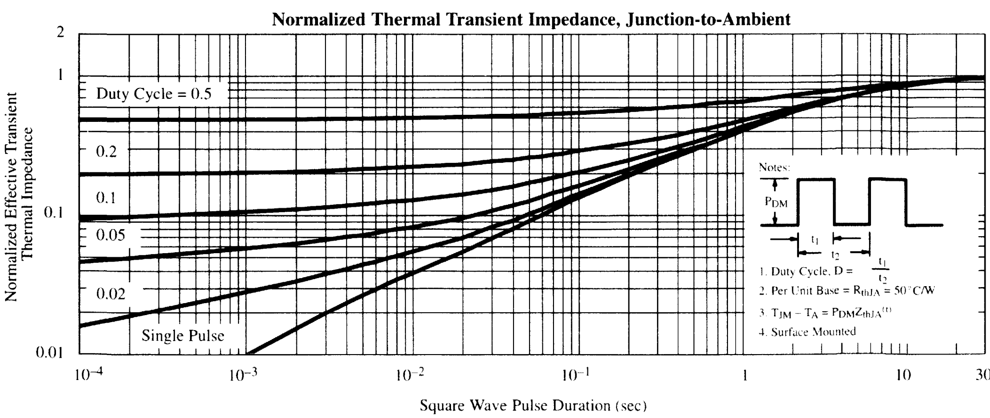
Typical Characteristics (25 °C Unless Otherwise Noted)









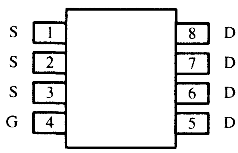


P-Channel Enhancement-Mode MOSFET

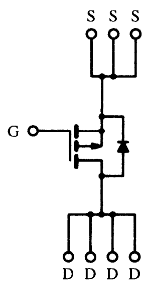
Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
–30	0.02 @ V_{GS} = –10 V	± 8.0
	0.035 @ V_{GS} = –4.5 V	± 6.0

SO-8



Top View



P-Channel MOSFET

Absolute Maximum Ratings (T_A = 25 °C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	–30	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	± 8.0	A
	T_A = 70°C		± 6.4	
Pulsed Drain Current		I_{DM}	± 50	
Continuous Source Current (Diode Conduction)[a]		I_S	–2.1	
Maximum Power Dissipation[NO TAG]	T_A = 25°C	P_D	2.5	W
	T_A = 70°C		1.6	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient[a]	R_{thJA}	50	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 10 sec.

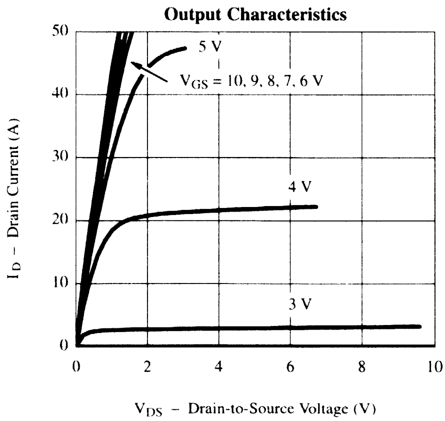
Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70149. A SPICE Model data sheet is available for this product (FaxBack document #70544).

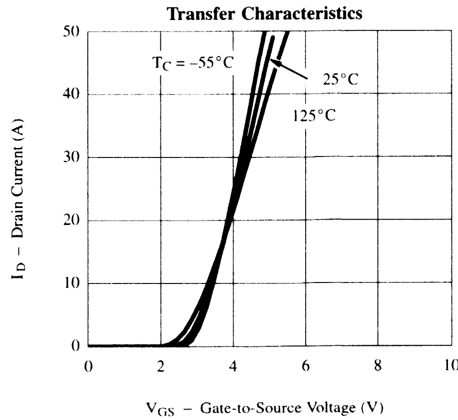
Specifications (T_J = 25°C Unless Otherwise Noted)

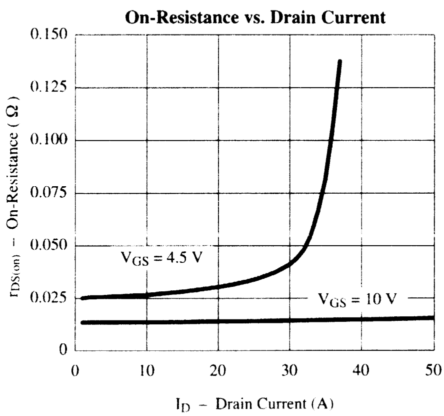
Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250\ \mu A$	-1.0			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = \pm 20$ V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -30$ V, $V_{GS} = 0$ V			-1	µA
		$V_{DS} = -15$ V, $V_{GS} = 0$ V, $T_J = 70°C$			-5	
On-State Drain Current[b]	$I_{D(on)}$	$V_{DS} \leq -5$ V, $V_{GS} = -10$ V	-20			A
		$V_{DS} \leq -5$ V, $V_{GS} = -4.5$ V	-10			
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	$V_{GS} = -10$ V, $I_D = -8.0$ A		0.014	0.02	Ω
		$V_{GS} = -4.5$ V, $I_D = -5.0$ A		0.026	0.035	
Forward Transconductance[b]	g_{fs}	$V_{DS} = -15$ V, $I_D = -8.0$ A		15		S
Diode Forward Voltage[b]	V_{SD}	$I_S = -2.1$ A, $V_{GS} = 0$ V		-0.77	-1.2	V
Dynamic[a]						
Total Gate Charge	Q_g	$V_{DS} = -15$ V, $V_{GS} = -10$ V, $I_D = -4.6$ A		44	60	nC
Gate-Source Charge	Q_{gs}			9		
Gate-Drain Charge	Q_{gd}			8		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -15$ V, $R_L = 15\ \Omega$ $I_D \cong -1$ A, $V_{GEN} = -10$ V, $R_G = 6\ \Omega$		15	30	ns
Rise Time	t_r			10	20	
Turn-Off Delay Time	$t_{d(off)}$			85	120	
Fall Time	t_f			45	80	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -2.1$ A, di/dt = 100 A/µs		60	100	

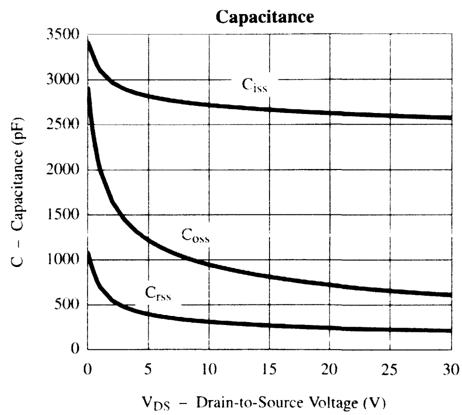
Notes
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

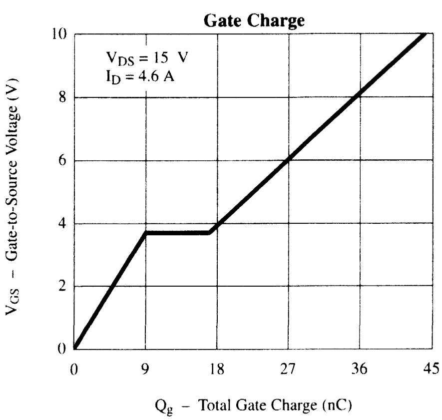
Typical Characteristics (25 °C Unless Noted)

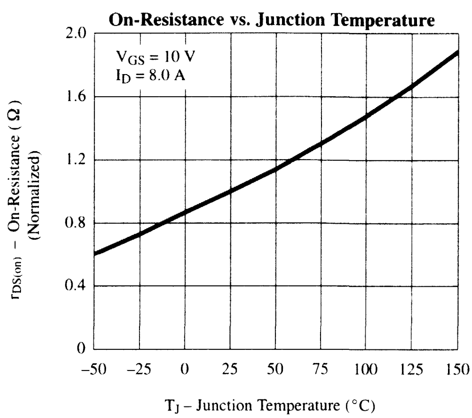






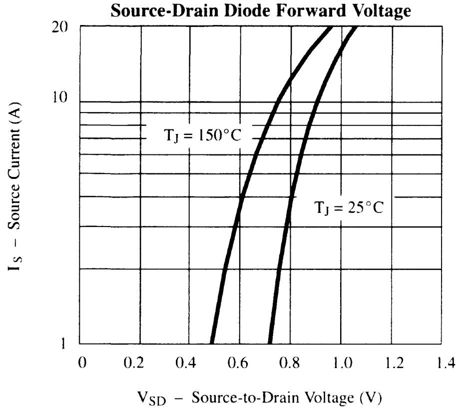




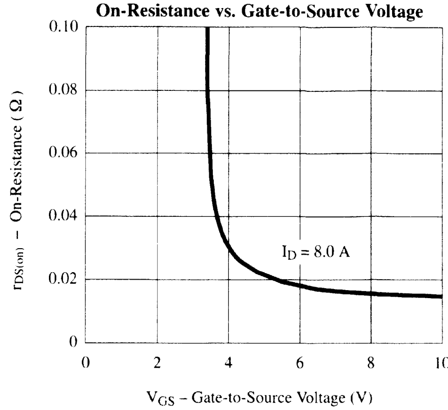


Typical Characteristics (25 °C Unless Otherwise Noted)

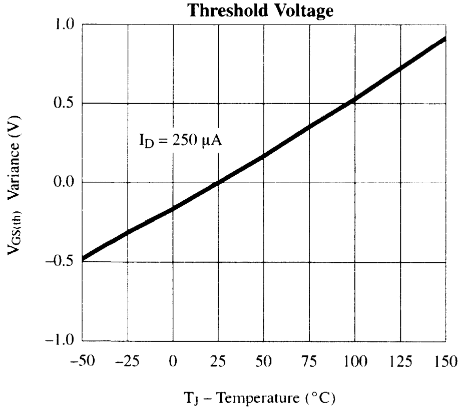
Source-Drain Diode Forward Voltage



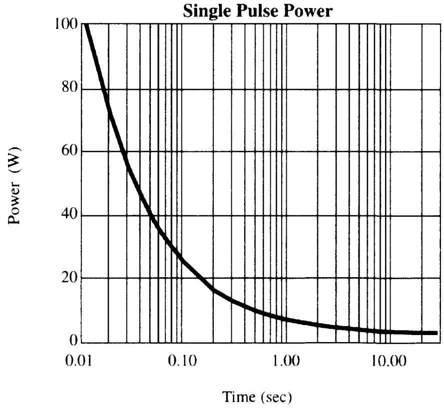
On-Resistance vs. Gate-to-Source Voltage



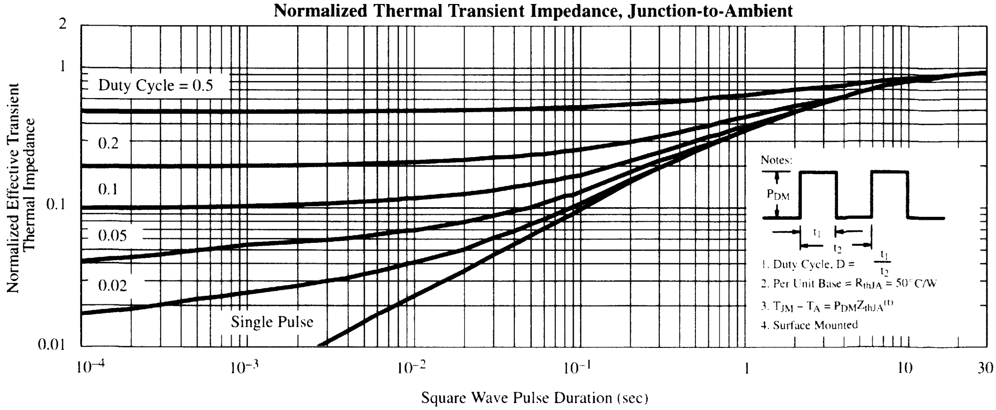
Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient

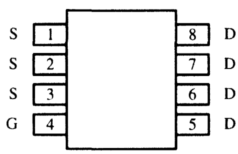


N-Channel Enhancement-Mode MOSFET

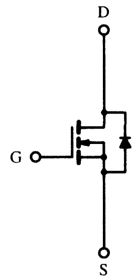
Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
60	0.024 @ V_{GS} = 10 V	±7.5
	0.03 @ V_{GS} = 6.0 V	±6.5

SO-8



Top View



N-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	±7.5	A
	T_A = 70°C		±5.5	
Pulsed Drain Current		I_{DM}	±50	
Continuous Source Current (Diode Conduction)[a]		I_S	2.1	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	2.5	W
	T_A = 70°C		1.6	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient[a]	R_{thJA}	50	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70144.

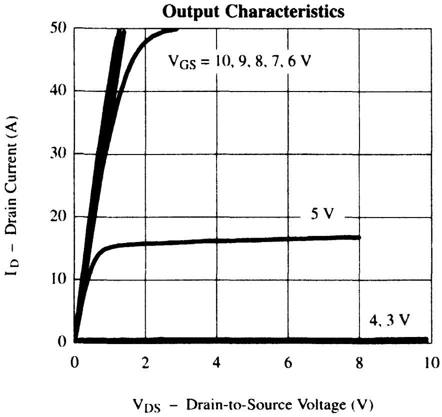
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 µA	2			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60 V, V_{GS} = 0 V			1	µA
		V_{DS} = 60 V, V_{GS} = 0 V, T_J = 55°C			20	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 10 V	20			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 7.5 A		0.020	0.024	Ω
		V_{GS} = 6.0 V, I_D = 6.5 A		0.025	0.03	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 7.5 A		18.5		S
Diode Forward Voltage[b]	V_{SD}	I_S = 2.1 A, V_{GS} = 0 V		0.75	1.2	V
Dynamic						
Total Gate Charge	Q_g	V_{DS} = 30 V, V_{GS} = 10 V, I_D = 7.5 A		31	50	nC
Gate-Source Charge	Q_{gs}			7.7		
Gate-Drain Charge	Q_{gd}			8.3		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 30 V, R_L = 30 Ω I_D ≅ 1 A, V_{GEN} = 10 V, R_G = 6 Ω		16	30	ns
Rise Time	t_r			11	20	
Turn-Off Delay Time	$t_{d(off)}$			41	80	
Fall Time	t_f			21	40	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 2.1 A, di/dt = 100 A/µs		46	80	

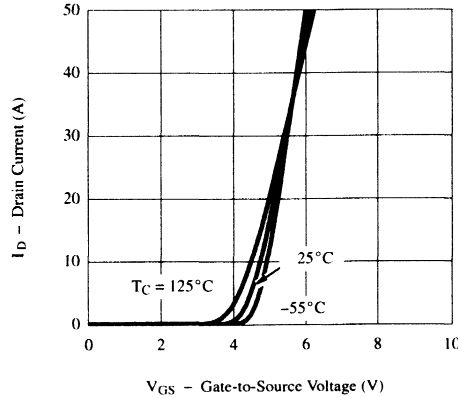
Notes
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

Typical Characteristics (25 °C Unless Otherwise Noted)

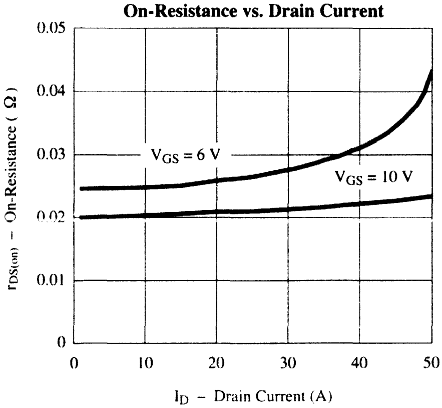
Output Characteristics



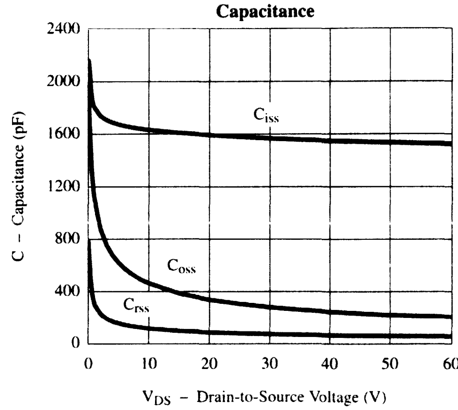
Transfer Characteristics



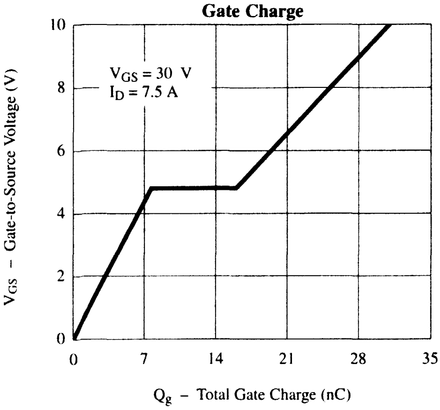
On-Resistance vs. Drain Current



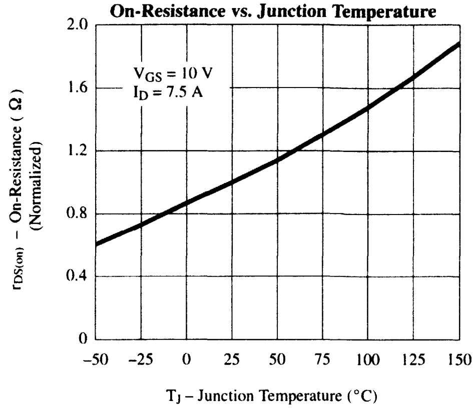
Capacitance



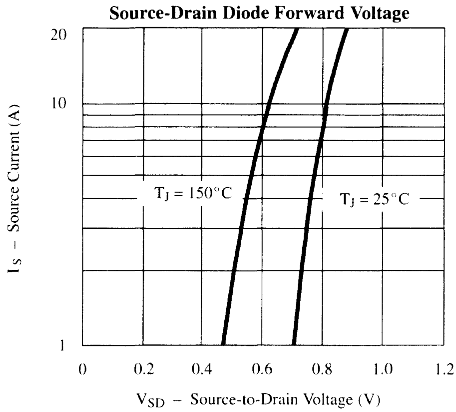
Gate Charge

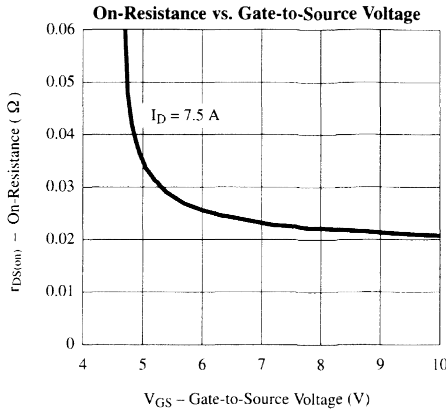


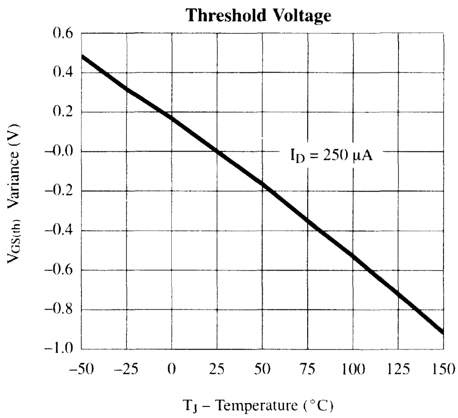
On-Resistance vs. Junction Temperature

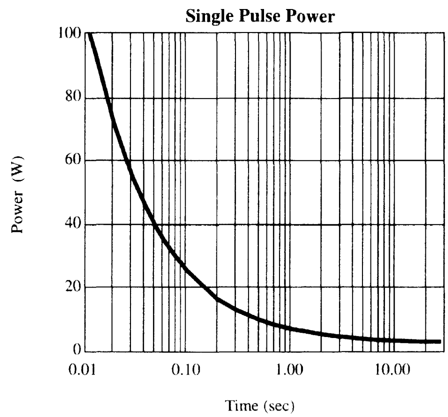


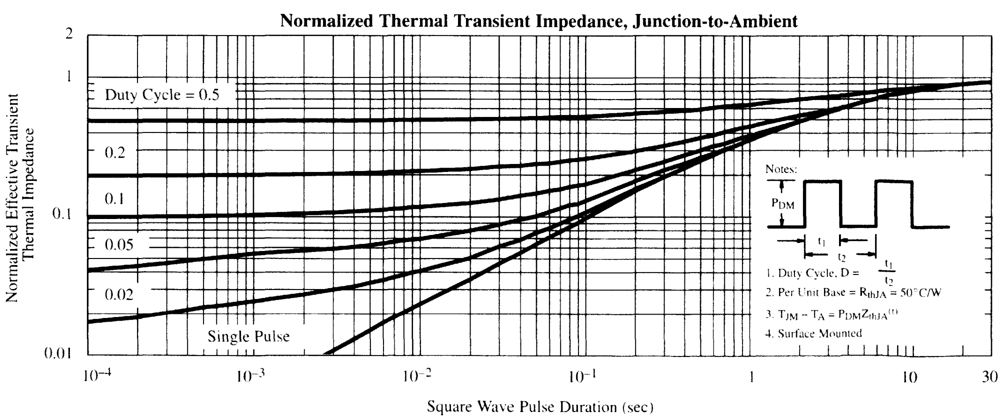
Typical Characteristics (25°C Unless Otherwise Noted)











N-Channel 80-V Rated MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
80	0.035 @ V_{GS} = 10 V	± 6.0
	0.040 @ V_{GS} = 6.0 V	± 5.5

TrenchFET™ Power MOSFETS

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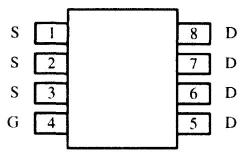
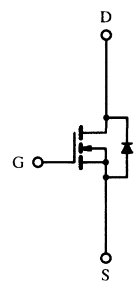


Top View



N-Channel MOSFET

Absolute Maximum Ratings (T_A = 25 °C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	80	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 150 °C)[a]	T_A = 25 °C	I_D	± 6.0	A
	T_A = 70 °C		± 48	
Pulsed Drain Current		I_{DM}	± 40	
Continuous Source Current (Diode Conduction)[a]		I_S	2.1	
Maximum Power Dissipation[a]	T_A = 25 °C	P_D	2.5	W
	T_A = 70 °C		1.6	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient[a]	R_{thJA}	50	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 10 sec.

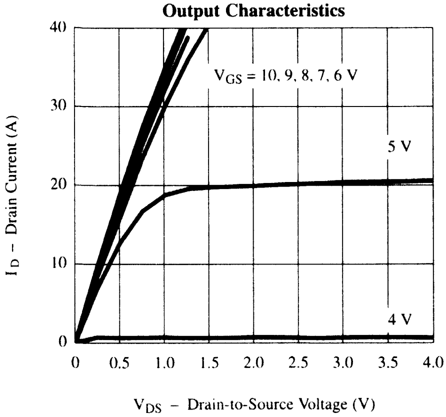
Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70645.

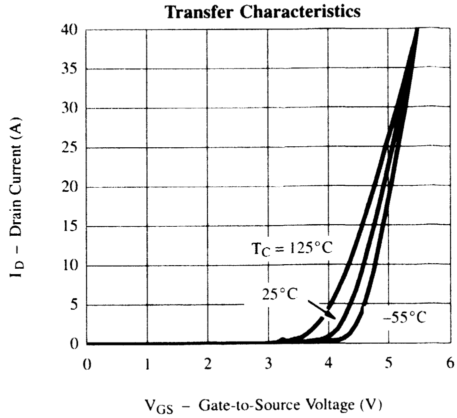
Specifications (T_J = 25°C Unless Otherwise Noted)

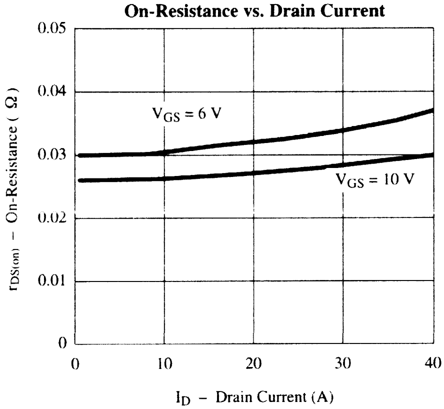
Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 µA	2			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80 V, V_{GS} = 0 V			1	µA
		V_{DS} = 80 V, V_{GS} = 0 V, T_J = 55°C			20	
On-State Drain Curren[b]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 10 V	20			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 6.0 A		0.026	0.035	Ω
		V_{GS} = 6.0 V, I_D = 5.5 A		0.030	0.040	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 6.0 A		25		S
Diode Forward Voltage[b]	V_{SD}	I_S = 2.1 A, V_{GS} = 0 V			1.2	V
Dynamic[a]						
Total Gate Charge	Q_g	V_{DS} = 40 V, V_{GS} = 10 V, I_D = 6.0 A		30	50	nC
Gate-Source Charge	Q_{gs}			9		
Gate-Drain Charge	Q_{gd}			5.6		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 40 V, R_L = 30 Ω I_D ≅ 1 A, V_{GEN} = 10 V, R_G = 6 Ω		12.5	25	ns
Rise Time	t_r			12.5	25	
Turn-Off Delay Time	$t_{d(off)}$			52	80	
Fall Time	t_f			22	40	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 2.1 A, di/dt = 100 A/µs		50	80	

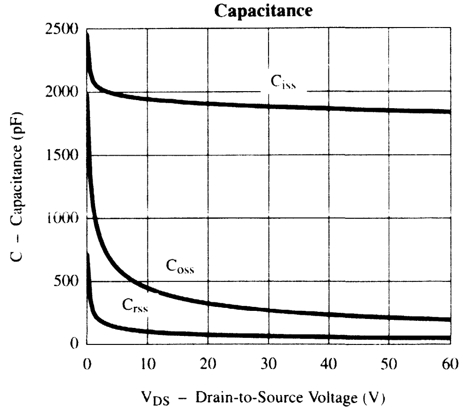
Notes
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

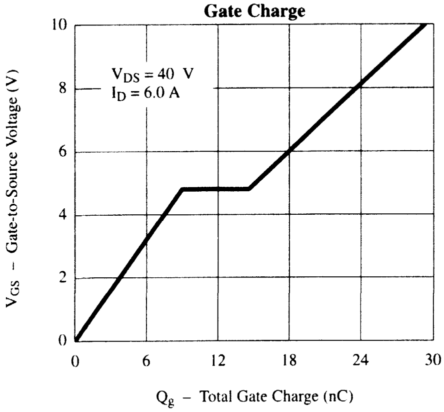
Typical Characteristics (25 °C Unless Otherwise Noted)

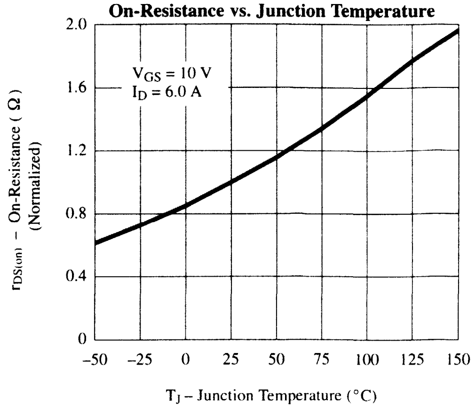






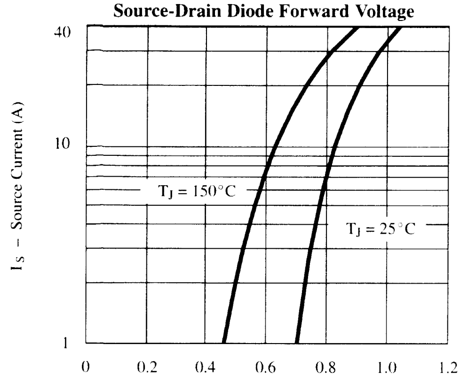


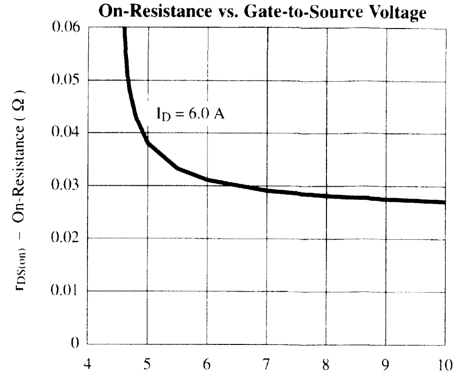


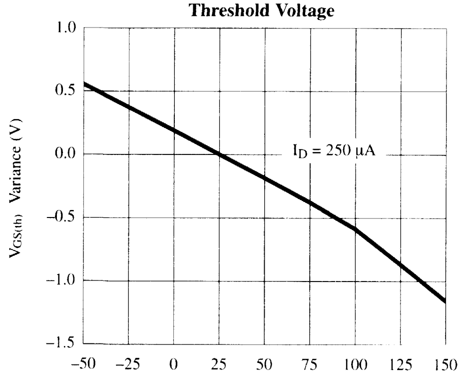


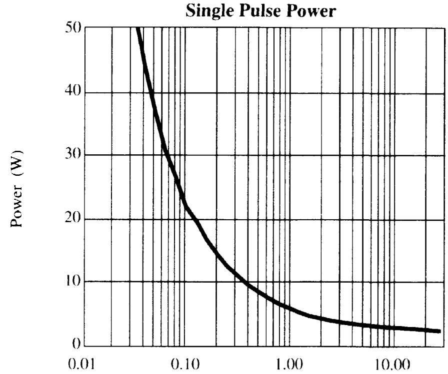
New Product

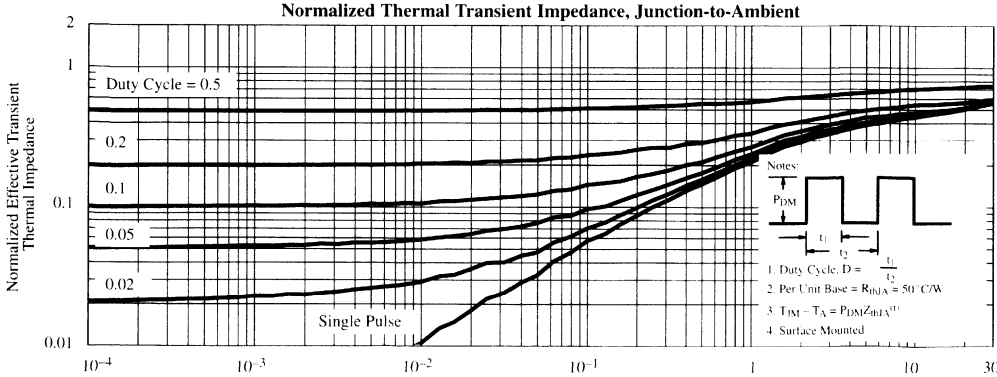
Typical Characteristics (25°C Unless Otherwise Noted)











New Product

Dual N- and P-Channel 30-V (D-S) Rated MOSFET

Product Summary

	V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
N-Channel	30	0.065 @ V_{GS} = 10 V	± 3.9
		0.095 @ V_{GS} = 4.5 V	± 3.1
P-Channel	–30	0.085 @ V_{GS} = –10 V	± 3.5
		0.19 @ V_{GS} = –4.5 V	± 2.5

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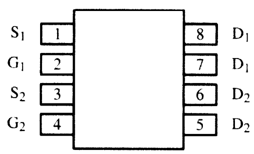
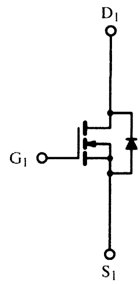
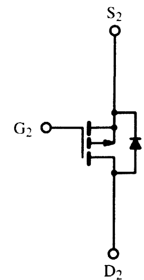


Top View



N-Channel MOSFET



P-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage		V_{DS}	30	–30	V
Gate-Source Voltage		V_{GS}	± 20	± 20	
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	± 3.9	± 3.5	A
	T_A = 70°C		± 3.1	± 2.8	
Pulsed Drain Current		I_{DM}	± 20	± 20	
Continuous Source Current (Diode Conduction)[a]		I_S	1.7	–1.7	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	2.0		W
	T_A = 70°C		1.3		
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150		°C

Thermal Resistance Ratings

Parameter	Symbol	N- or P-Channel	Unit
Maximum Junction-to-Ambient[a]	R_{thJA}	62.5	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 10 sec.

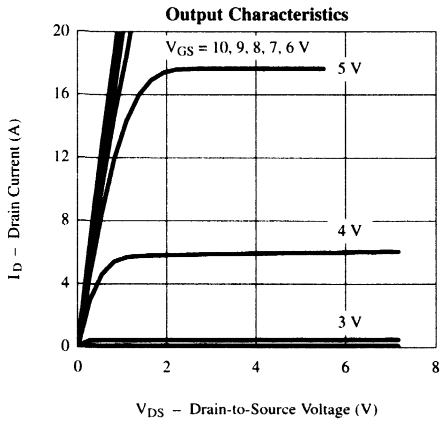
Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70155. A SPICE Model data sheet is available for this product (FaxBack document #70551)

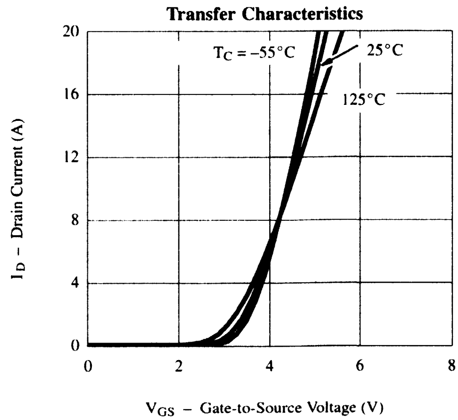
Specifications (T_J = 25°C Unless Otherwise Noted)

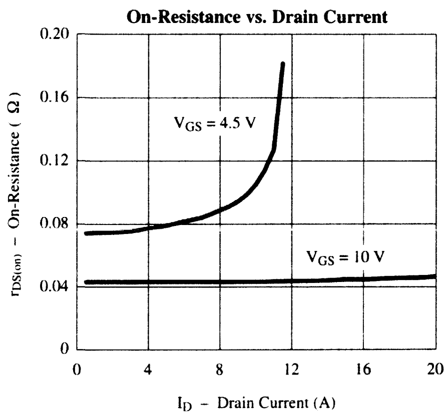
Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Static							
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 µA	N-Ch	1.0			V
		$V_{DS} = V_{GS}$, I_D = −250 µA	P-Ch	−1.0			
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V	N-Ch			± 100	nA
			P-Ch			± 100	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V	N-Ch			1	µA
		V_{DS} = −30 V, V_{GS} = 0 V	P-Ch			−1	
		V_{DS} = 30 V, V_{GS} = 0 V, T_J = 55°C	N-Ch			25	
		V_{DS} = −30 V, V_{GS} = 0 V, T_J = 55°C	P-Ch			−25	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 10 V	N-Ch	15			A
		V_{DS} ≥ −5 V, V_{GS} = −10 V	P-Ch	−15			
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 3.9 A	N-Ch		0.043	0.065	Ω
		V_{GS} = −10 V, I_D = 2.5 A	P-Ch		0.066	0.085	
		V_{GS} = 4.5 V, I_D = 3.1 A	N-Ch		0.075	0.095	
		V_{GS} = −4.5 V, I_D = 1.8 A	P-Ch		0.125	0.19	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 3.9 A	N-Ch		7		S
		V_{DS} = −15 V, I_D = − 2.5 A	P-Ch		5		
Diode Forward Voltage[b]	V_{SD}	I_S = 1.7 A, V_{GS} = 0 V	N-Ch		0.8	1.2	V
		I_S = −1.7 A, V_{GS} = 0 V	P-Ch		−0.8	−1.2	
Dynamic[a]							
Total Gate Charge	Q_g	N-Channel V_{DS} = 10 V, V_{GS} = 10 V, I_D = 3.9 A P-Channel V_{DS} = −10 V, V_{GS} = −10 V, I_D = −2.5 A	N-Ch		9.8	15	nC
			P-Ch		8.7	15	
Gate-Source Charge	Q_{gs}		N-Ch		2.1		
			P-Ch		1.9		
Gate-Drain Charge	Q_{gd}		N-Ch		1.6		
			P-Ch		1.3		
Turn-On Delay Time	$t_{d(on)}$	N-Channel V_{DD} = 10 V, R_L = 10 Ω I_D ≅ 1 A, V_{GEN} = 10 V, R_G = 6 Ω P-Channel V_{DD} = −10 V, R_L = 10 Ω I_D ≅ −1 A, V_{GEN} = −10 V, R_G = 6 Ω	N-Ch		9	15	ns
			P-Ch		7	15	
Rise Time	t_r		N-Ch		6	18	
			P-Ch		9	18	
Turn-Off Delay Time	$t_{d(off)}$		N-Ch		18	27	
			P-Ch		14	27	
Fall Time	t_f		N-Ch		6	15	
			P-Ch		8	15	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 1.7 A, di/dt = 100 A/µs	N-Ch		52	80	
		I_F = −1.7 A, di/dt = 100 A/µs	P-Ch		50	80	

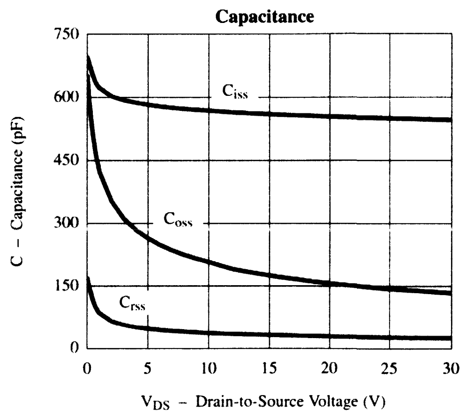
Notes
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

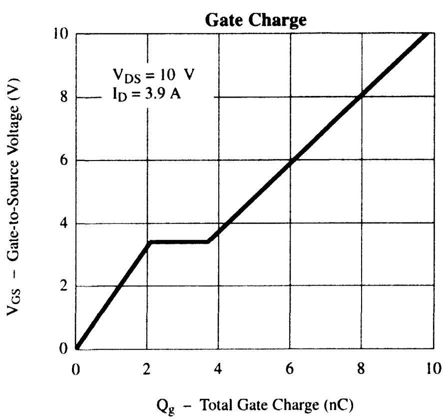
Typical Characteristics (25 °C Unless Noted) N-Channel

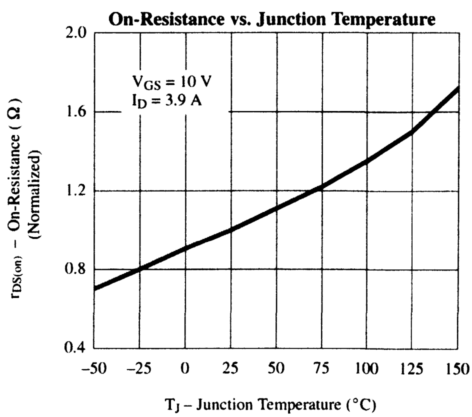












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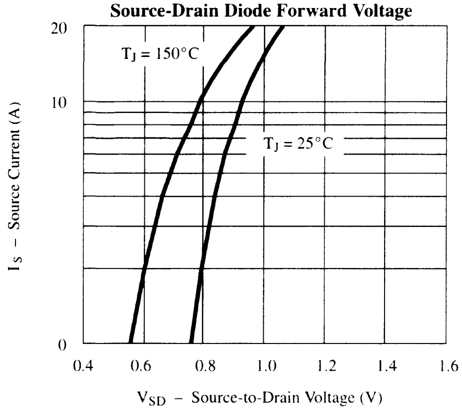
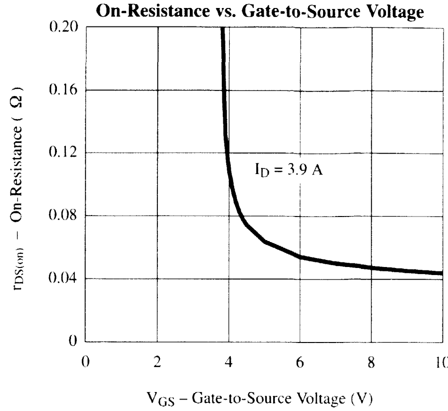
SOIC-8

Typical Characteristics (25°C Unless Noted) — N-Channel

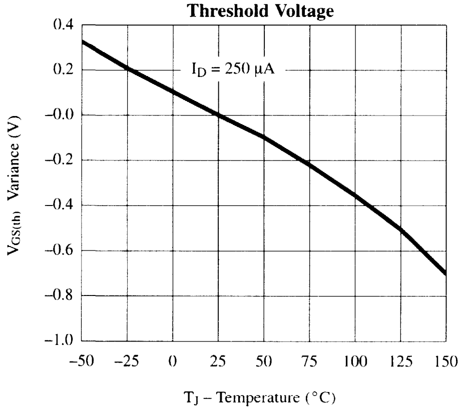
Source-Drain Diode Forward Voltage



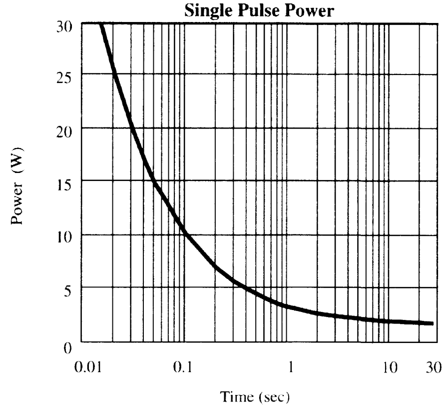
On-Resistance vs. Gate-to-Source Voltage



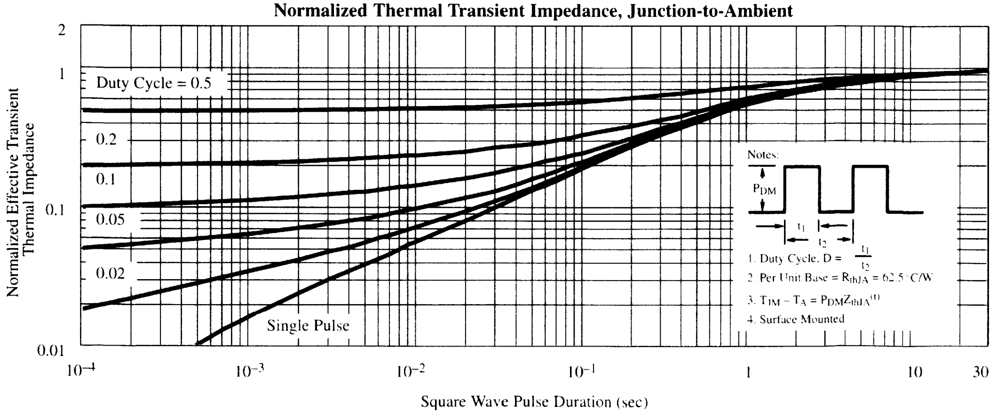
Threshold Voltage



Single Pulse Power

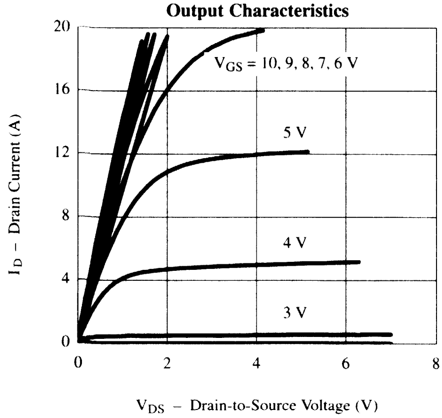


Normalized Thermal Transient Impedance, Junction-to-Ambient

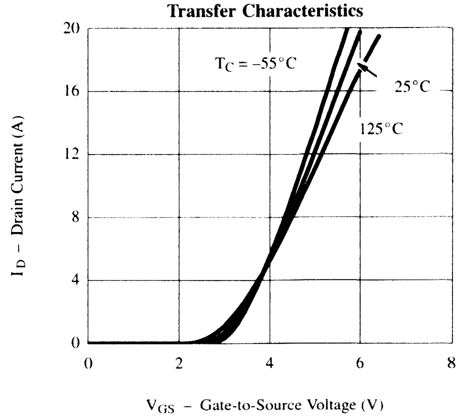


Typical Characteristics (25°C Unless Noted) P-Channel

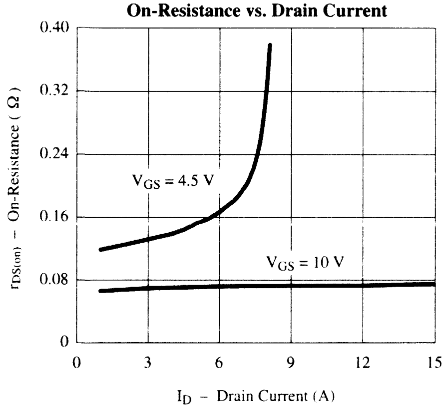
Output Characteristics



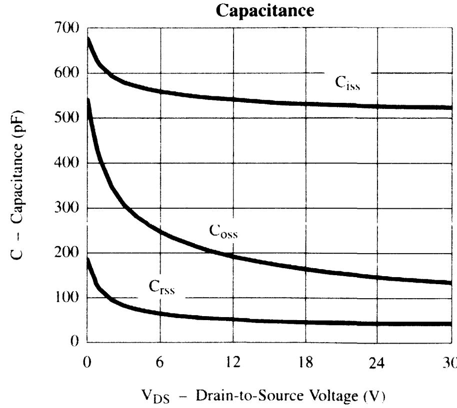
Transfer Characteristics



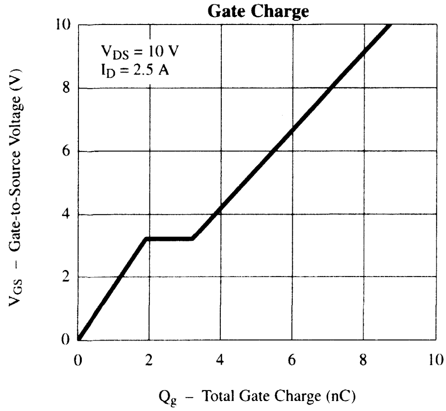
On-Resistance vs. Drain Current



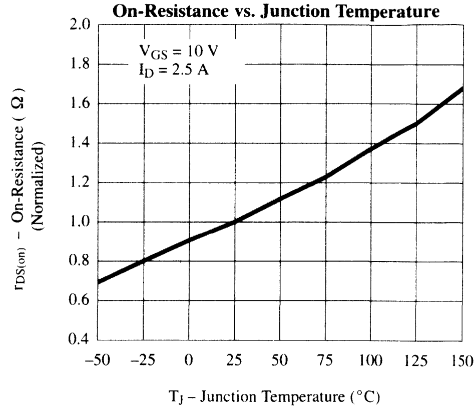
Capacitance



Gate Charge



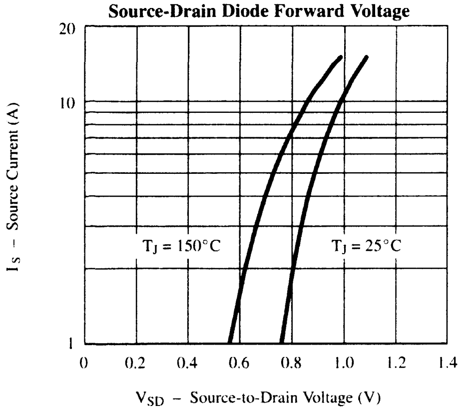
On-Resistance vs. Junction Temperature



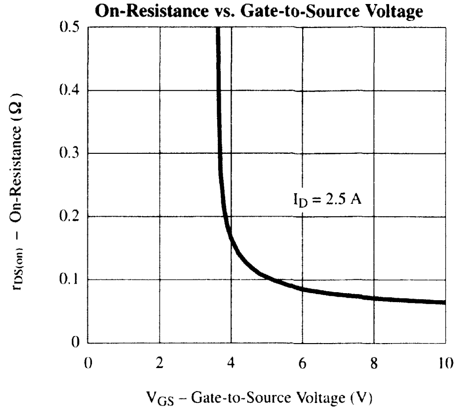
Typical Characteristics (25 °C Unless Noted)

P-Channel

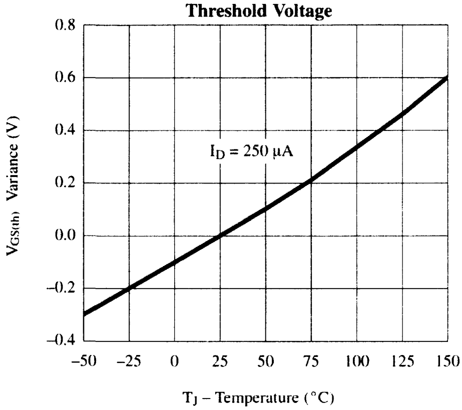
Source-Drain Diode Forward Voltage



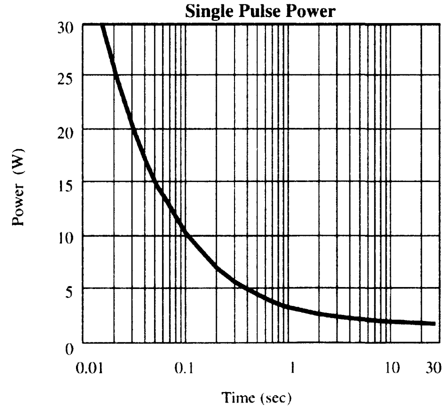
On-Resistance vs. Gate-to-Source Voltage



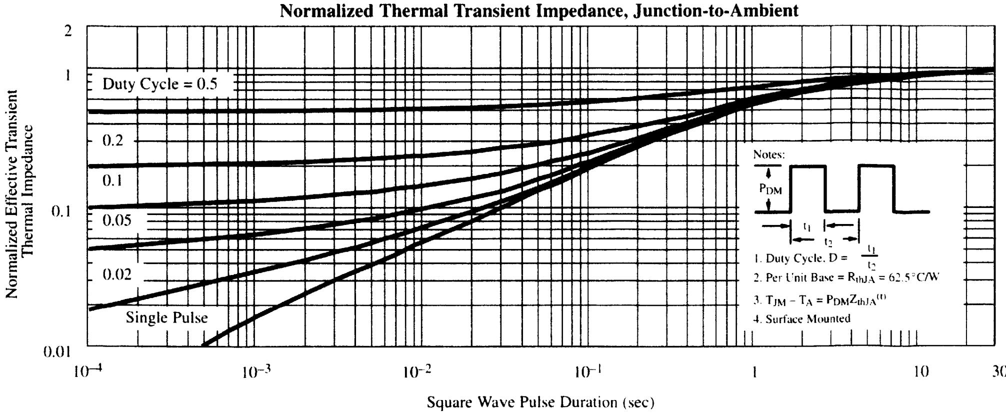
Threshold Voltage



Single Pulse Power



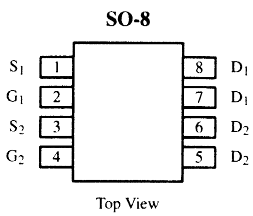
Normalized Thermal Transient Impedance, Junction-to-Ambient

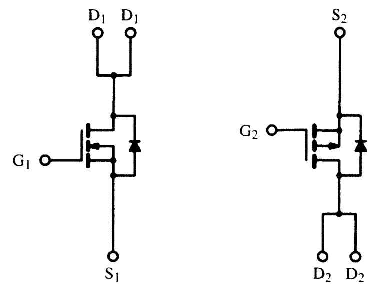


Dual Enhancement-Mode MOSFET (N- and P-Channel)

Product Summary

	V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
N-Channel	30	0.037 @ V_{GS} = 10 V	±5.8
		0.055 @ V_{GS} = 4.5 V	±4.7
P-Channel	–30	0.053 @ V_{GS} = –10 V	±4.9
		0.095 @ V_{GS} = –4.5 V	±3.6





N-Channel MOSFET

P-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage		V_{DS}	30	–30	V
Gate-Source Voltage		V_{GS}	±20	±20	
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	±5.8	±4.9	A
	T_A = 70°C		±4.6	±3.9	
Pulsed Drain Current		I_{DM}	±30	±30	
Continuous Source Current (Diode Conduction)[a]		I_S	1.7	–1.7	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	2.0	2.0	W
	T_A = 70°C		1.3	1.3	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150		°C

Thermal Resistance Ratings

Parameter	Symbol	N- or P-Channel	Unit
Maximum Junction-to-Ambient[a]	R_{thJA}	62.5	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 10 sec.

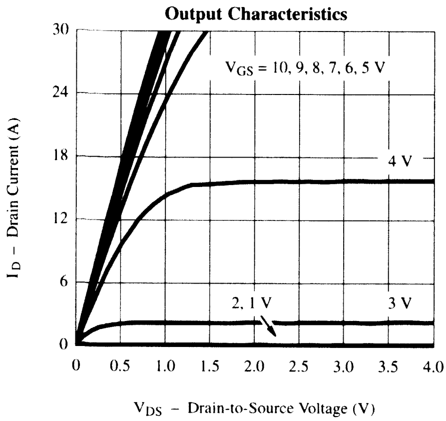
Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70152.
A SPICE Model data sheet is available for this product (FaxBack document #70555).

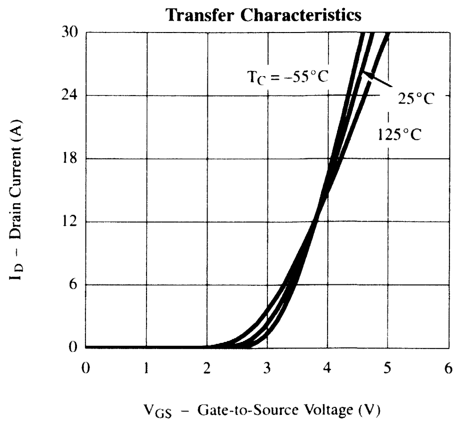
Specifications (T_J = 25°C Unless Otherwise Noted)

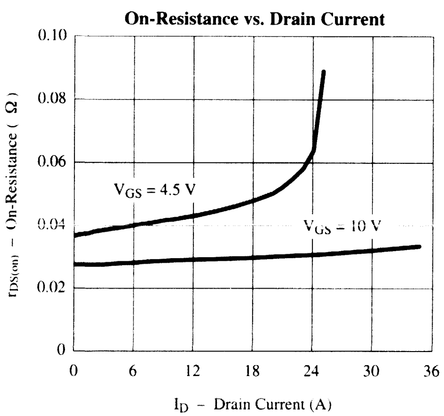
Parameter	Symbol	Test Condition		Min	Typ[a]	Max	Unit
Static							
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\ \mu A$	N-Ch	1.0			V
		$V_{DS} = V_{GS}$, $I_D = -250\ \mu A$	P-Ch	−1.0			
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = \pm 20$ V	N-Ch			± 100	nA
			P-Ch			± 100	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30$ V, $V_{GS} = 0$ V	N-Ch			1	µA
		$V_{DS} = -30$ V, $V_{GS} = 0$ V	P-Ch			−1	
		$V_{DS} = 30$ V, $V_{GS} = 0$ V, $T_J = 55°C$	N-Ch			25	
		$V_{DS} = -30$ V, $V_{GS} = 0$ V, $T_J = 55°C$	P-Ch			−25	
On-State Drain Current[b]	$I_{D(on)}$	$V_{DS} \geq 5$ V, $V_{GS} = 10$ V	N-Ch	20			A
		$V_{DS} \leq -5$ V, $V_{GS} = -10$ V	P-Ch	−20			
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	$V_{GS} = 10$ V, $I_D = 5.8$ A	N-Ch		0.030	0.037	Ω
		$V_{GS} = -10$ V, $I_D = -4.9$ A	P-Ch		0.043	0.053	
		$V_{GS} = 4.5$ V, $I_D = 4.7$ A	N-Ch		0.042	0.055	
		$V_{GS} = -4.5$ V, $I_D = -3.6$ A	P-Ch		0.070	0.095	
Forward Transconductance[b]	g_{fs}	$V_{DS} = 15$ V, $I_D = 5.8$ A	N-Ch		13		S
		$V_{DS} = -15$ V, $I_D = -4.9$ A	P-Ch		10		
Diode Forward Voltage[b]	V_{SD}	$I_S = 1.7$ A, $V_{GS} = 0$ V	N-Ch		0.8	1.2	V
		$I_S = -1.7$ A, $V_{GS} = 0$ V	P-Ch		−0.8	−1.2	
Dynamic[a]							
Total Gate Charge	Q_g	N-Channel $V_{DS} = 15$ V, $V_{GS} = 10$ V, $I_D = 5.8$ A P-Channel $V_{DS} = -15$ V, $V_{GS} = -10$ V, $I_D = -4.9$ A	N-Ch		18	25	nC
			P-Ch		16	25	
Gate-Source Charge	Q_{gs}		N-Ch		4.5		
			P-Ch		5		
Gate-Drain Charge	Q_{gd}		N-Ch		2.5		
			P-Ch		2		
Turn-On Delay Time	$t_{d(on)}$	N-Channel $V_{DD} = 15$ V, $R_L = 15\ \Omega$ $I_D \cong 1$ A, $V_{GEN} = 10$ V, $R_G = 6\ \Omega$ P-Channel $V_{DD} = -15$ V, $R_L = 15\ \Omega$ $I_D \cong -1$ A, $V_{GEN} = -10$ V, $R_G = 6\ \Omega$	N-Ch		10	16	ns
			P-Ch		9	15	
Rise Time	t_r		N-Ch		20	16	
			P-Ch		13	20	
Turn-Off Delay Time	$t_{d(off)}$		N-Ch		27	40	
			P-Ch		25	40	
Fall Time	t_f		N-Ch		24	35	
			P-Ch		15	25	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 1.7$ A, di/dt = 100 A/µs	N-Ch		45	80	
		$I_F = -1.7$ A, di/dt = 100 A/µs	P-Ch		60	90	

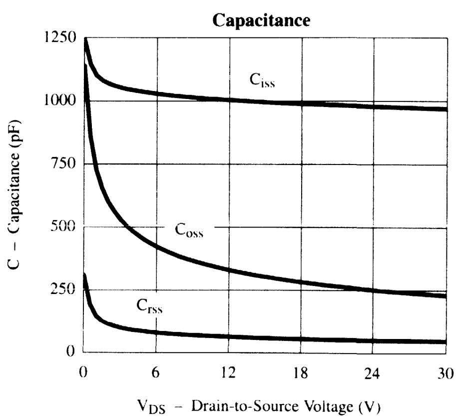
Notes
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

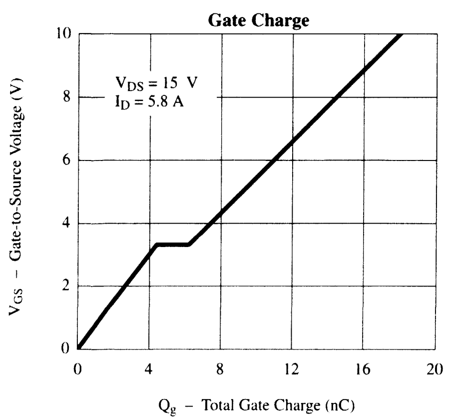
Typical Characteristics (25°C Unless Noted) N-Channel

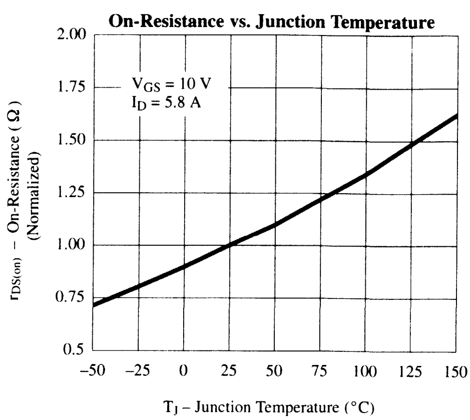






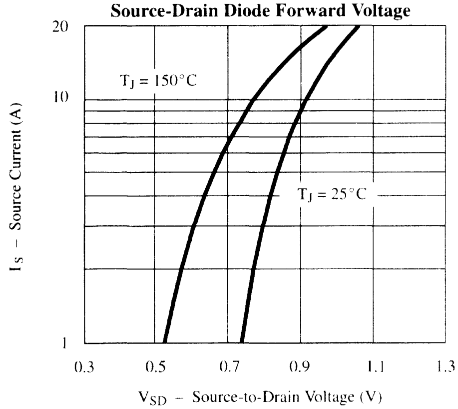




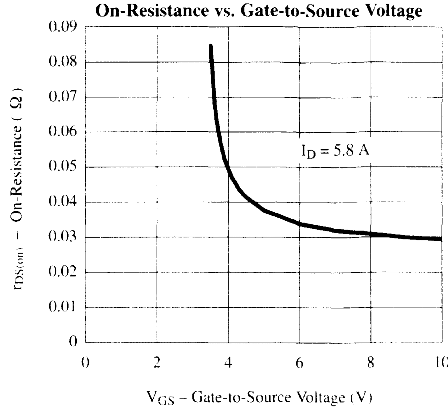


Typical Characteristics (25°C Unless Noted) N-Channel

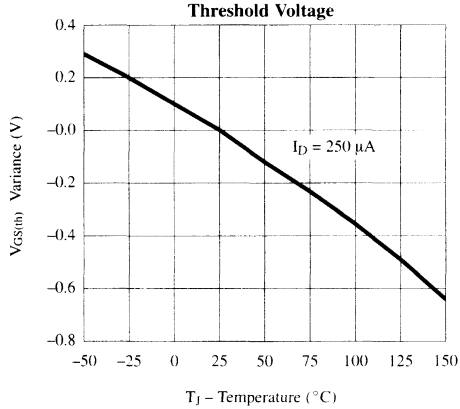
Source-Drain Diode Forward Voltage



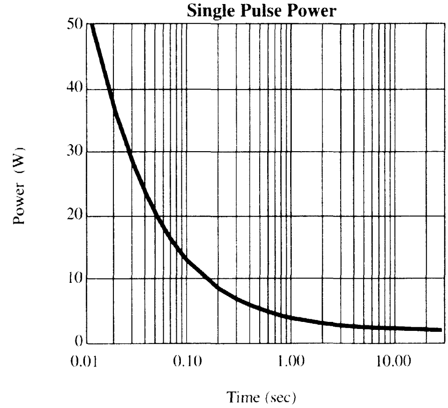
On-Resistance vs. Gate-to-Source Voltage



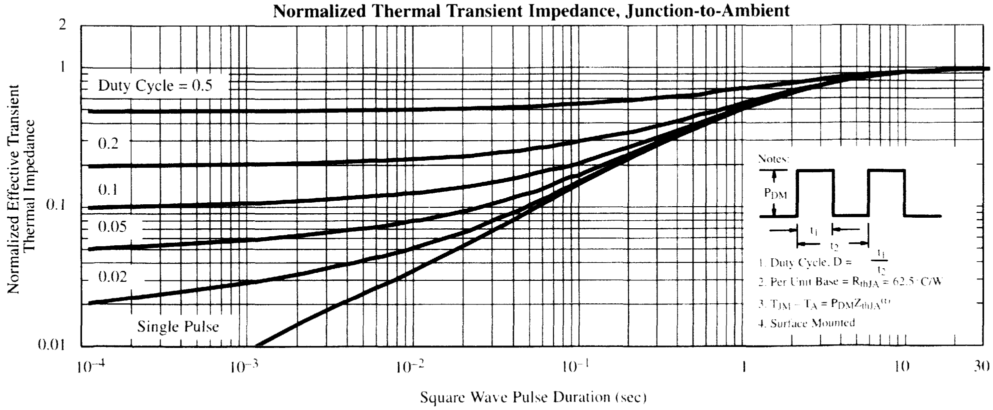
Threshold Voltage



Single Pulse Power

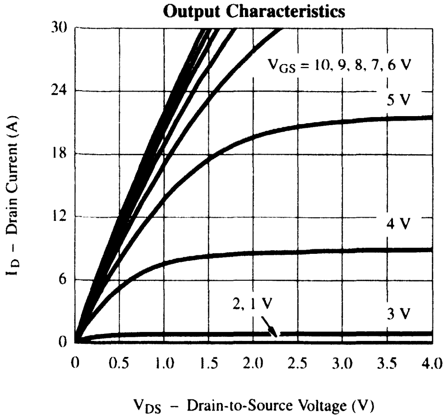


Normalized Thermal Transient Impedance, Junction-to-Ambient

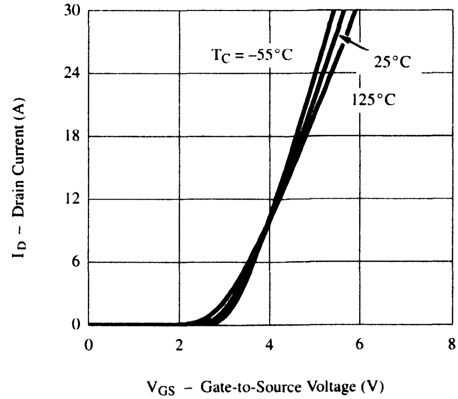


Typical Characteristics (25°C Unless Noted) P-Channel

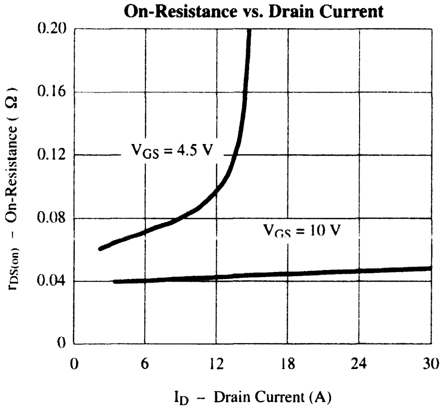
Output Characteristics



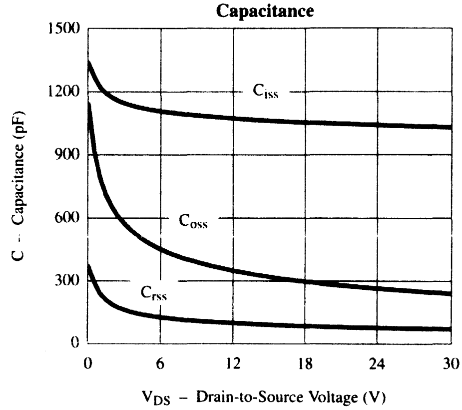
Transfer Characteristics



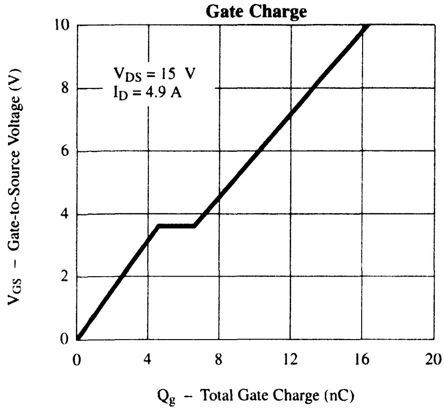
On-Resistance vs. Drain Current



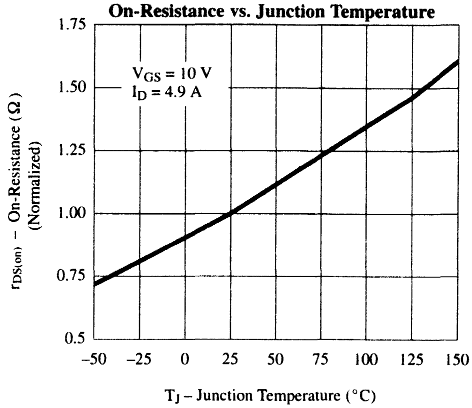
Capacitance



Gate Charge

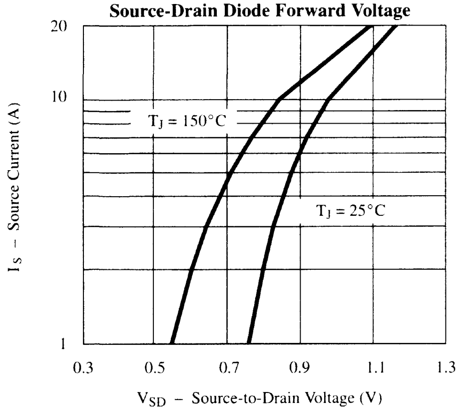


On-Resistance vs. Junction Temperature

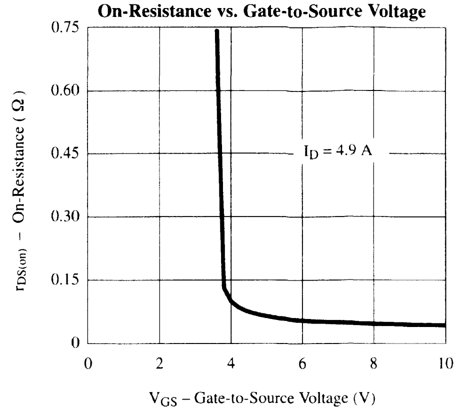


Typical Characteristics (25 °C Unless Noted) — P-Channel

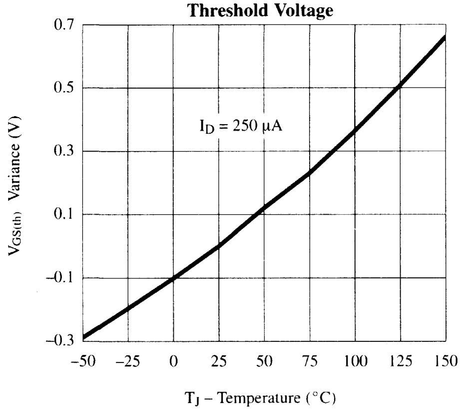
Source-Drain Diode Forward Voltage



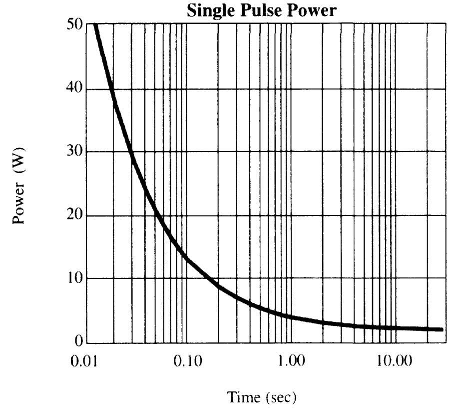
On-Resistance vs. Gate-to-Source Voltage



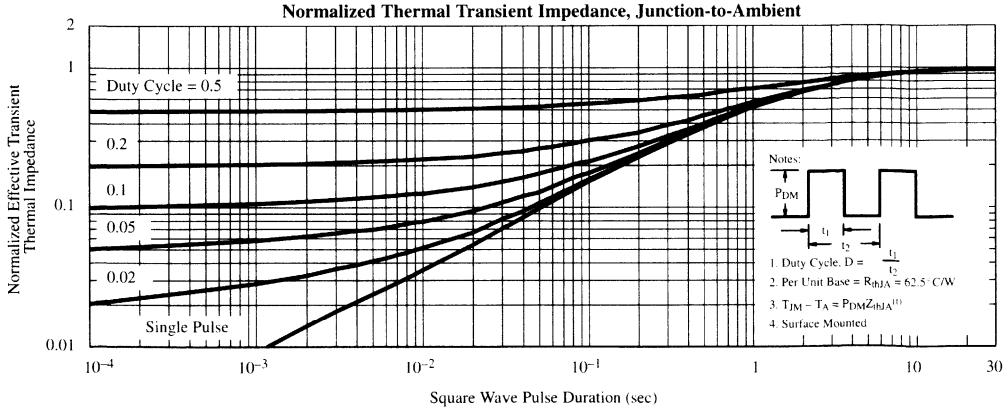
Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient



Dual N- and P-Channel 60-V, 175°C Rated MOSFET

Product Summary

	V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
N-Channel	60	0.055 @ V_{GS} = 10 V	±4.5
		0.075 @ V_{GS} = 4.5 V	±3.9
P-Channel	–60	0.120 @ V_{GS} = –10 V	±3.1
		0.150 @ V_{GS} = –4.5 V	±2.8

175°C Rated Maximum Junction Temperature
TrenchFET™ Power MOSFETs

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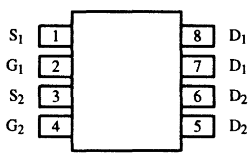
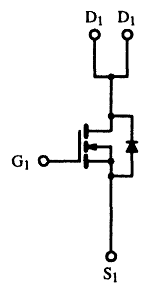
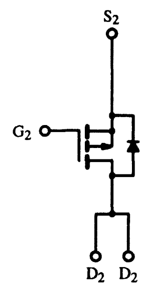


Top View



N-Channel MOSFET



P-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage		V_{DS}	60	–60	V
Gate-Source Voltage		V_{GS}	±20	±20	
Continuous Drain Current (T_J = 175°C)[a]	T_A = 25°C	I_D	±4.5	±3.1	A
	T_A = 70°C		±3.8	±2.6	
Pulsed Drain Current		I_{DM}	±30	±30	
Continuous Source Current (Diode Conduction)[a]		I_S	2.0	–2.0	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	2.4		W
	T_A = 70°C		1.7		
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 175		°C

Thermal Resistance Ratings

Parameter	Symbol	N- or P- Channel	Unit
Maximum Junction-to-Ambient[a]	R_{thJA}	62.5	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 10 sec.

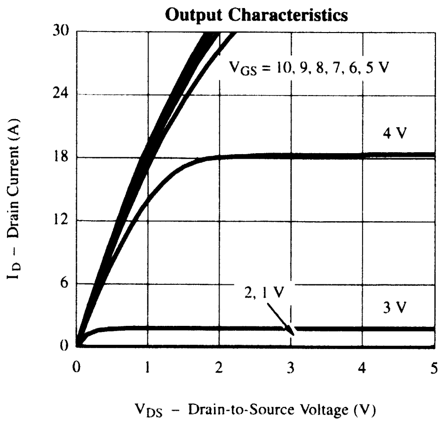
Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70167.

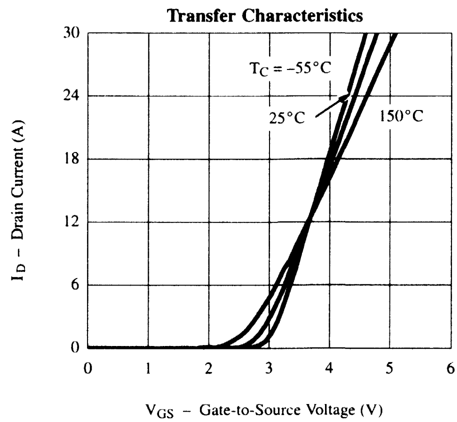
Specifications ($T_J = 25°C$ Unless Otherwise Noted)

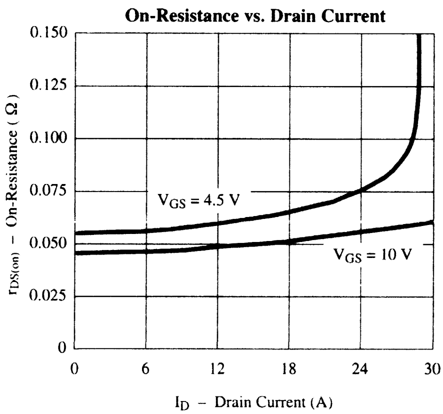
Parameter	Symbol	Test Condition		Min	Typ[a]	Max	Unit
Static							
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\ \mu A$	N-Ch	1			V
		$V_{DS} = V_{GS}$, $I_D = -250\ \mu A$	P-Ch	−1			
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = \pm 20$ V	N-Ch			± 100	nA
			P-Ch			± 100	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 60$ V, $V_{GS} = 0$ V	N-Ch			2	μA
		$V_{DS} = -60$ V, $V_{GS} = 0$ V	P-Ch			−2	
		$V_{DS} = 60$ V, $V_{GS} = 0$ V, $T_J = 55°C$	N-Ch			25	
		$V_{DS} = -60$ V, $V_{GS} = 0$ V, $T_J = 55°C$	P-Ch			−25	
On-State Drain Current[b]	$I_{D(on)}$	$V_{DS} \geq 5$ V, $V_{GS} = 10$ V	N-Ch	20			A
		$V_{DS} \leq -5$ V, $V_{GS} = -10$ V	P-Ch	−20			
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	$V_{GS} = 10$ V, $I_D = 4.5$ A	N-Ch		0.045	0.055	Ω
		$V_{GS} = -10$ V, $I_D = -3.1$ A	P-Ch		0.100	0.120	
		$V_{GS} = 4.5$ V, $I_D = 3.9$ A	N-Ch		0.055	0.075	
		$V_{GS} = -4.5$ V, $I_D = -2.8$ A	P-Ch		0.125	0.150	
Forward Transconductance[b]	g_{fs}	$V_{DS} = 15$ V, $I_D = 4.5$ A	N-Ch		13		S
		$V_{DS} = -15$ V, $I_D = -3.1$ A	P-Ch		7.5		
Diode Forward Voltage[b]	V_{SD}	$I_S = 2.0$ A, $V_{GS} = 0$ V	N-Ch		0.9	1.2	V
		$I_S = -2.0$ A, $V_{GS} = 0$ V	P-Ch		−0.8	−1.2	
Dynamic[a]							
Total Gate Charge	Q_g	N-Channel $V_{DS} = 30$ V, $V_{GS} = 10$ V, $I_D = 4.5$ A; P-Channel $V_{DS} = -30$ V, $V_{GS} = -10$ V $I_D = -3.1$A	N-Ch		19	30	nC
			P-Ch		16	25	
Gate-Source Charge	Q_{gs}		N-Ch		4		
			P-Ch		4		
Gate-Drain Charge	Q_{gd}		N-Ch		3		
			P-Ch		1.6		
Turn-On Delay Time	$t_{d(on)}$	N-Channel $V_{DD} = 30$ V, $R_L = 30\ \Omega$ $I_D \cong 1$ A, $V_{GEN} = 10$ V, $R_G = 6\ \Omega$; P-Channel $V_{DD} = -30$ V, $R_L = 30\ \Omega$ $I_D \cong -1$ A, $V_{GEN} = -10$ V, $R_G = 6\ \Omega$	N-Ch		13	20	ns
			P-Ch		8	15	
Rise Time	t_r		N-Ch		11	20	
			P-Ch		10	20	
Turn-Off Delay Time	$t_{d(off)}$		N-Ch		36	60	
			P-Ch		12	25	
Fall Time	t_f		N-Ch		11	20	
			P-Ch		35	50	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 2$ A, di/dt = 100 A/μs	N-Ch		35	60	
		$I_F = -2$ A, di/dt = 100 A/μs	P-Ch		60	90	

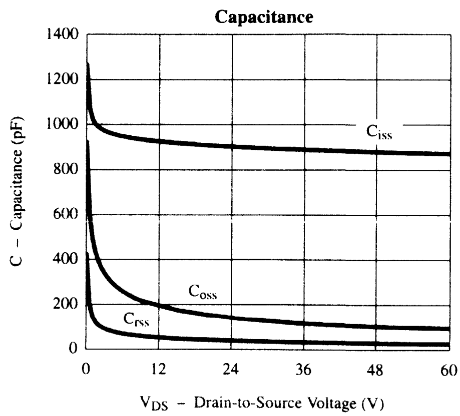
Notes
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.

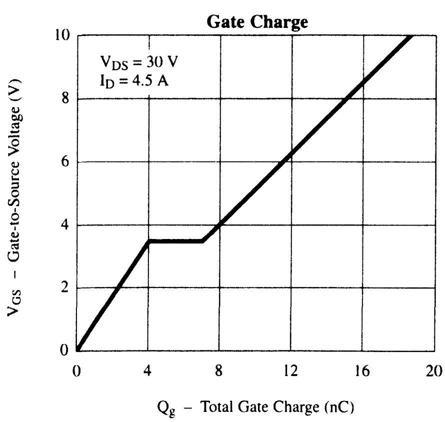
Typical Characteristics (25°C Unless Otherwise Noted) N-Channel

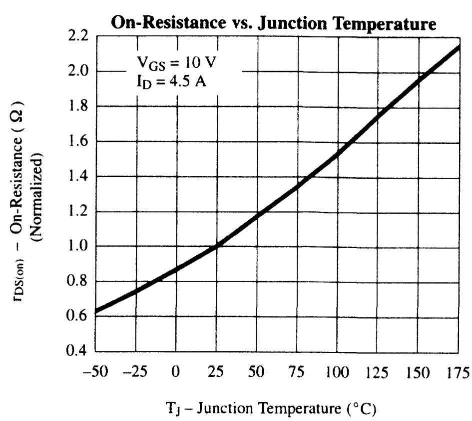












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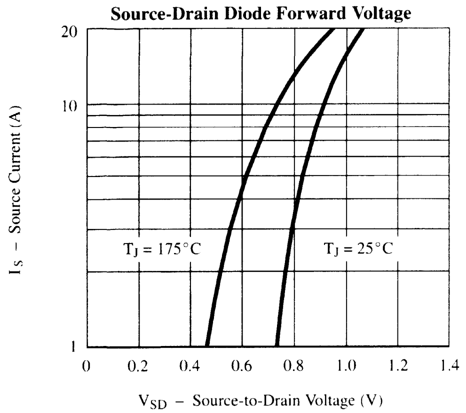
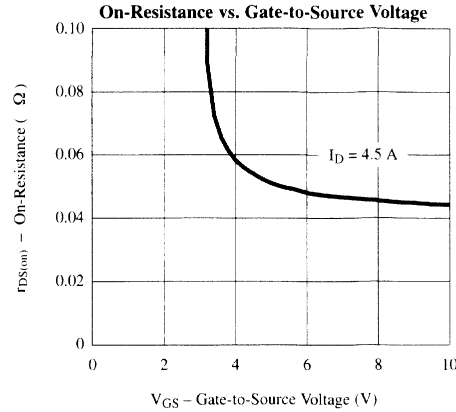
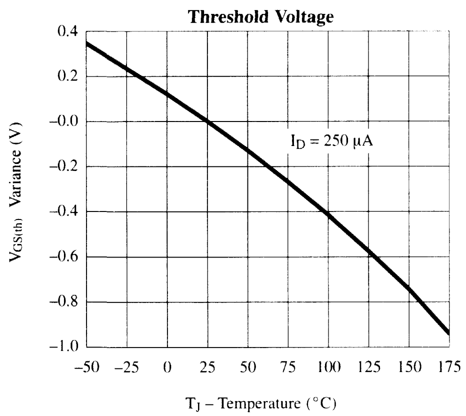
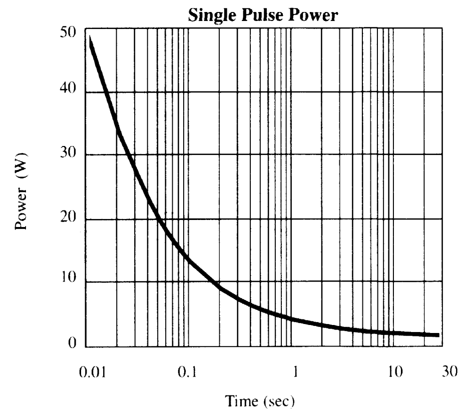
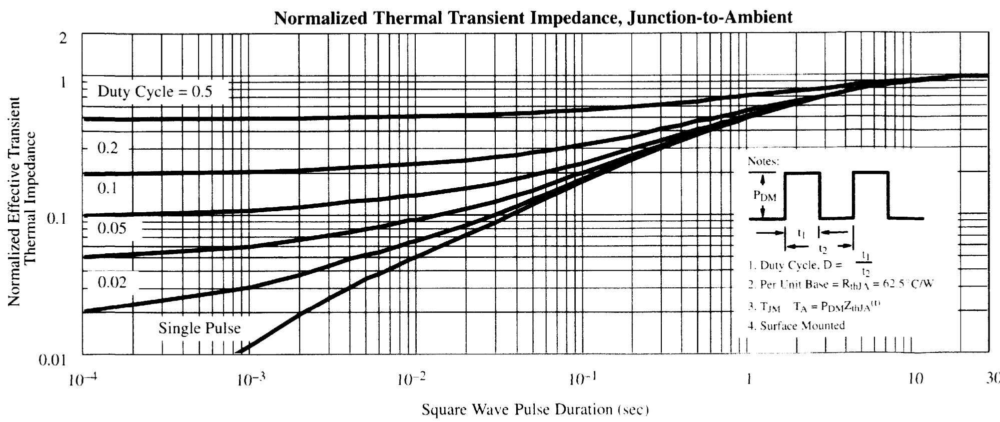
Typical Characteristics (25°C Unless Otherwise Noted) N-Channel





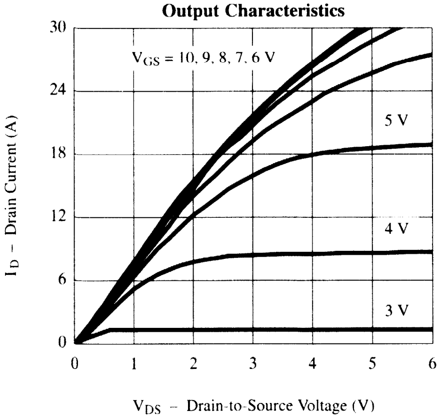




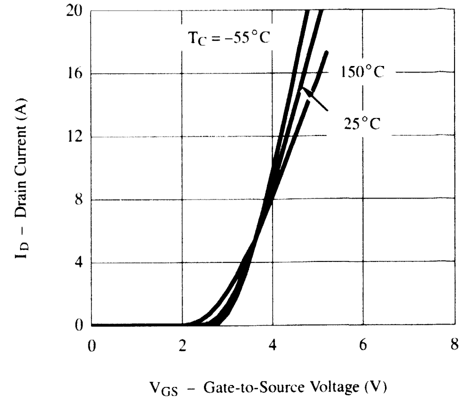


Typical Characteristics (25°C Unless Noted) — P-Channel

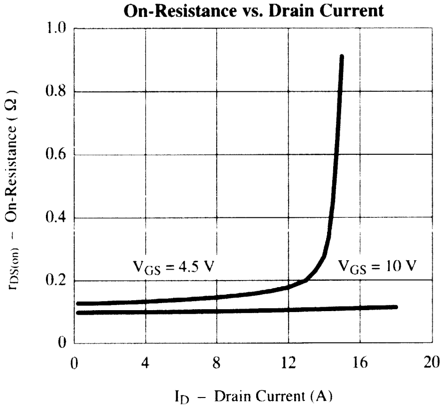
Output Characteristics



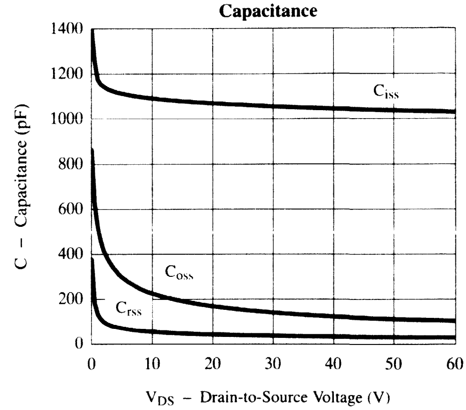
Transfer Characteristics



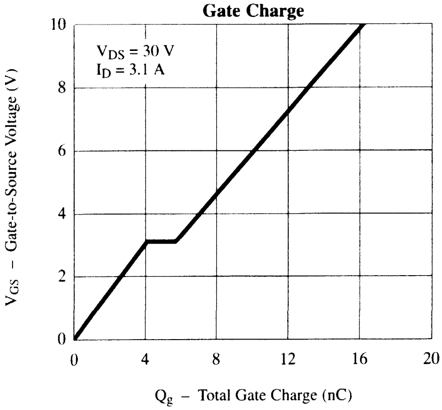
On-Resistance vs. Drain Current



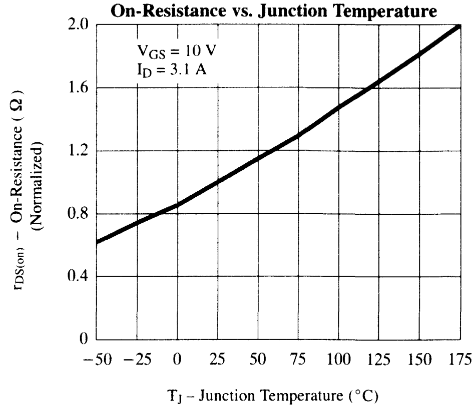
Capacitance



Gate Charge

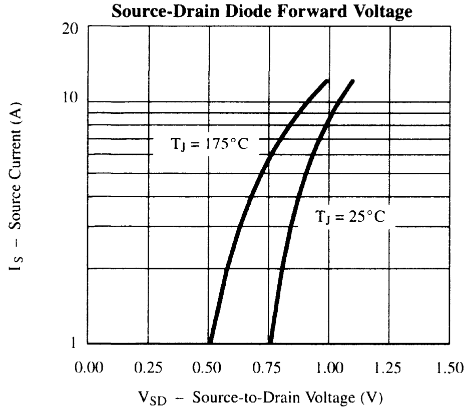


On-Resistance vs. Junction Temperature

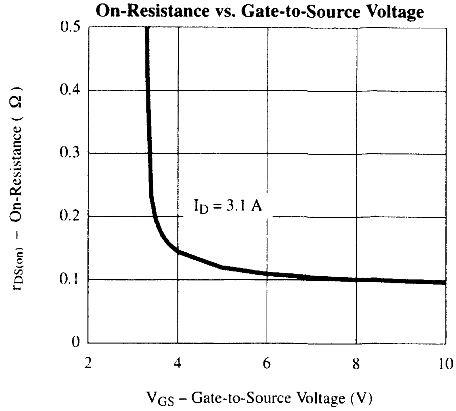


Typical Characteristics (25°C Unless Noted) P-Channel

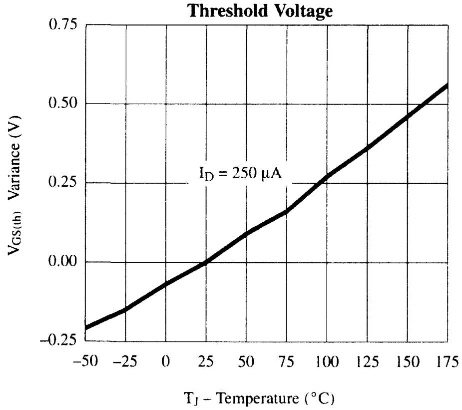
Source-Drain Diode Forward Voltage



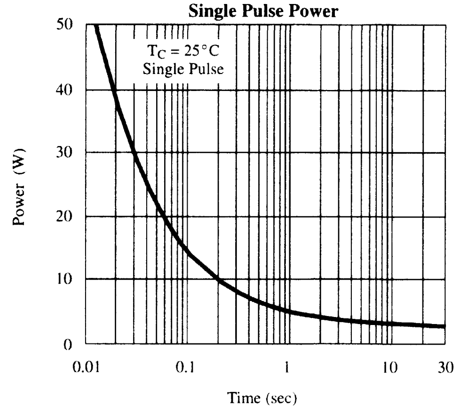
On-Resistance vs. Gate-to-Source Voltage



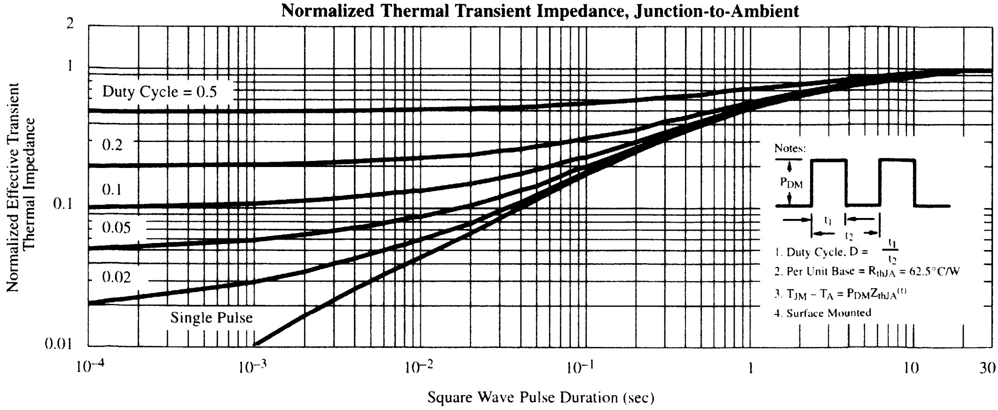
Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient



Si4902DY

Asymmetrical Dual N-Channel 30-V (D-S) Rated MOSFET

Product Summary

	V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
N-Channel 1	30	0.065 @ V_{GS} = 10 V	±3.0
		0.095 @ V_{GS} = 4.5 V	±2.5
N-Channel 2		0.028 @ V_{GS} = 10 V	±6.7
		0.042 @ V_{GS} = 4.5 V	±5.4

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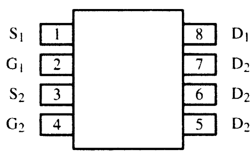
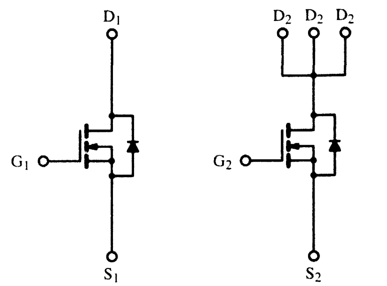


Top View



N-Channel MOSFET 1 N-Channel MOSFET 2

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	N-Channel 1	N-Channel 2	Unit
Drain-Source Voltage		V_{DS}	30	30	V
Gate-Source Voltage		V_{GS}	±20	±20	
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	±3.0	±6.7	A
	T_A = 70°C		±2.4	±5.4	
Pulsed Drain Current		I_{DM}	±20	±30	
Continuous Source Current (Diode Conduction)[a]		I_S	1.25	2.0	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	1.0	2.25	W
	T_A = 70°C		0.64	1.5	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	–55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	N-Channel 1	N-Channel 2	Unit
Maximum Junction-to-Ambient[a]	R_{thJA}	125	55	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70632. A SPICE Model data sheet is available for this product (FaxBack document #70561).

Specifications (T_J = 25°C Unless Otherwise Noted)

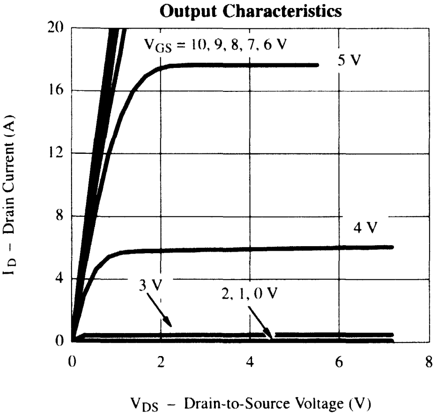
Parameter	Symbol	Test Condition		Min	Typ[a]	Max	Unit
Static							
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\ \mu A$	N-Ch 1	1.0			V
			N-Ch 2	1.0			
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = \pm 20$ V	N-Ch 1			± 100	nA
			N-Ch 2			± 100	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30$ V, $V_{GS} = 0$ V	N-Ch 1			1	μA
			N-Ch 2			1	
		$V_{DS} = 30$ V, $V_{GS} = 0$ V, $T_J = 55°C$	N-Ch 1			25	
			N-Ch 2			25	
On-State Drain Current[b]	$I_{D(on)}$	$V_{DS} \geq 5$ V, $V_{GS} = 10$ V	N-Ch 1	20			A
			N-Ch 2	30			
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	$V_{GS} = 10$ V, $I_D = 3.0$ A	N-Ch 1		0.043	0.065	Ω
		$V_{GS} = 10$ V, $I_D = 6.7$ A	N-Ch 2		0.021	0.028	
		$V_{GS} = 4.5$ V, $I_D = 2.5$ A	N-Ch 1		0.073	0.095	
		$V_{GS} = 4.5$ V, $I_D = 5.4$ A	N-Ch 2		0.032	0.042	
Forward Transconductance[b]	g_{fs}	$V_{DS} = 15$ V, $I_D = 3.0$ A	N-Ch 1		6.0		S
		$V_{DS} = 15$ V, $I_D = 6.7$ A	N-Ch 2		15.5		
Diode Forward Voltage[b]	V_{SD}	$I_S = 1.25$ A, $V_{GS} = 0$ V	N-Ch 1		0.75	1.2	V
		$I_S = 2.0$ A, $V_{GS} = 0$ V	N-Ch 2		0.8	1.2	
Dynamic[a]							
Total Gate Charge	Q_g	N-Channel 1 $V_{DS} = 15$ V, $V_{GS} = 10$ V, $I_D = 3.0$ A N-Channel 2 $V_{DS} = 15$ V, $V_{GS} = 10$ V, $I_D = 6.7$ A	N-Ch 1		10	15	nC
			N-Ch 2		24	30	
Gate-Source Charge	Q_{gs}		N-Ch 1		2.1		
			N-Ch 2		4.8		
Gate-Drain Charge	Q_{gd}		N-Ch 1		1.7		
			N-Ch 2		4.6		
Turn-On Delay Time	$t_{d(on)}$	N-Channel 1 $V_{DD} = 15$ V, $R_L = 15\ \Omega$ $I_D \cong 1$ A, $V_{GEN} = 10$ V, $R_G = 6\ \Omega$ N-Channel 2 $V_{DD} = 15$ V, $R_L = 15\ \Omega$ $I_D \cong 1$ A, $V_{GEN} = 10$ V, $R_G = 6\ \Omega$	N-Ch 1		10	15	ns
			N-Ch 2		14	20	
Rise Time	t_r		N-Ch 1		8	15	
			N-Ch 2		10	20	
Turn-Off Delay Time	$t_{d(off)}$		N-Ch 1		19	30	
			N-Ch 2		36	55	
Fall Time	t_f		N-Ch 1		8	15	
			N-Ch 2		12	20	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 1.25$ A, di/dt = 100 A/μs	N-Ch 1		45	80	
		$I_F = 2.0$ A, di/dt = 100 A/μs	N-Ch 2		48	80	

Notes
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.

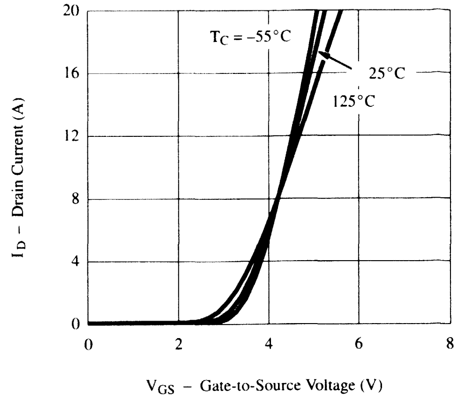
Typical Characteristics (25 °C Unless Noted)

N-Channel 1

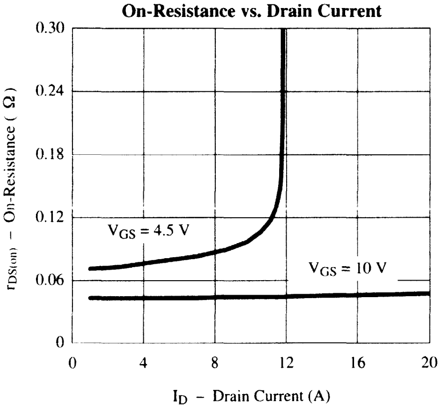
Output Characteristics



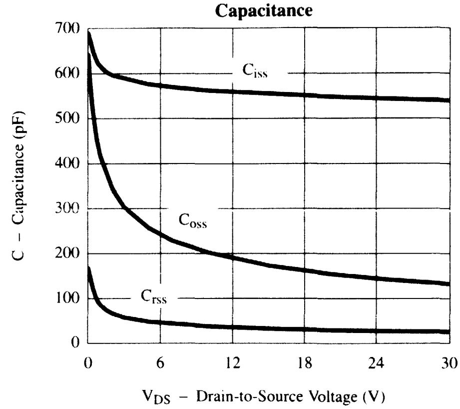
Transfer Characteristics



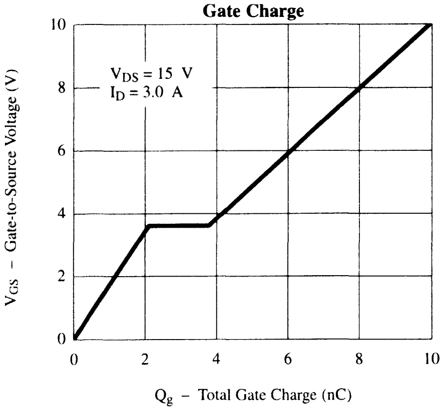
On-Resistance vs. Drain Current



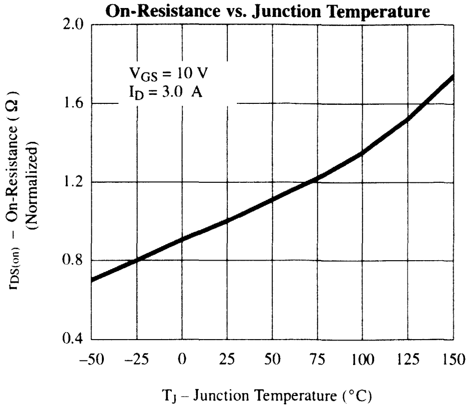
Capacitance



Gate Charge



On-Resistance vs. Junction Temperature



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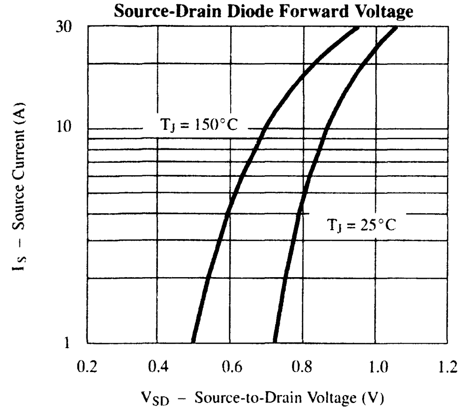
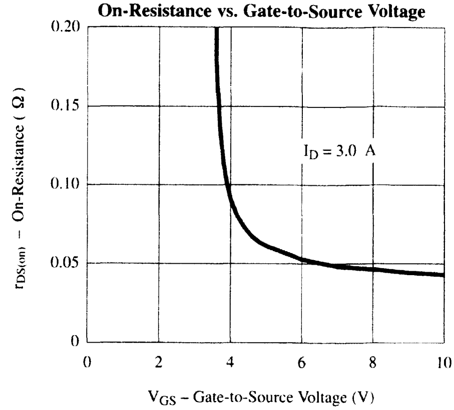
Typical Characteristics (25°C Unless Noted) — N-Channel 1

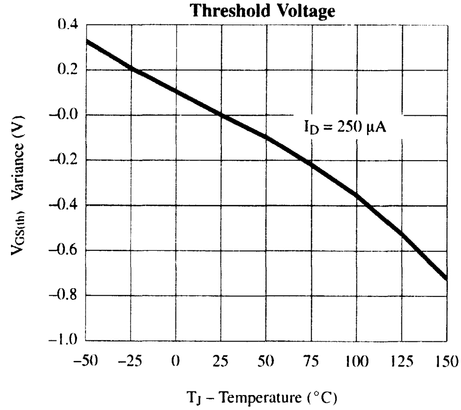
Source-Drain Diode Forward Voltage



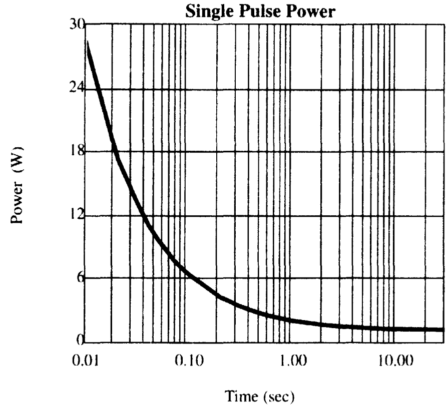
On-Resistance vs. Gate-to-Source Voltage



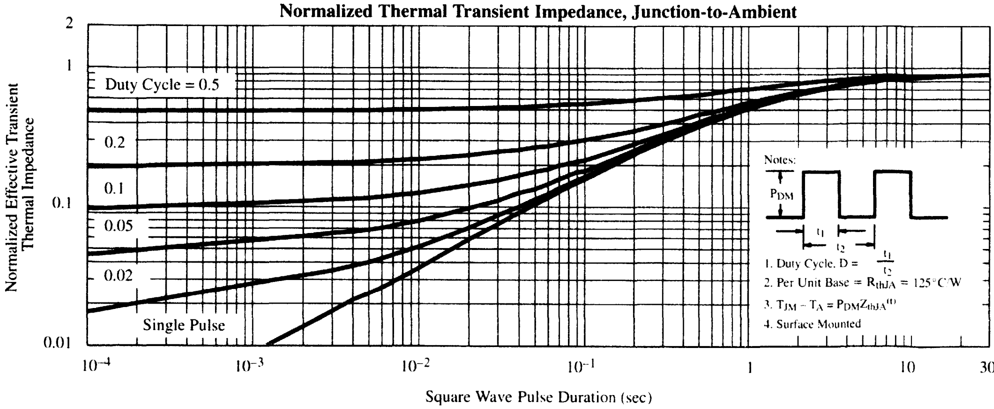
Threshold Voltage



Single Pulse Power

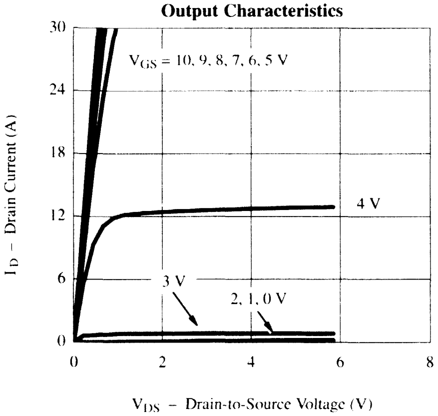


Normalized Thermal Transient Impedance, Junction-to-Ambient

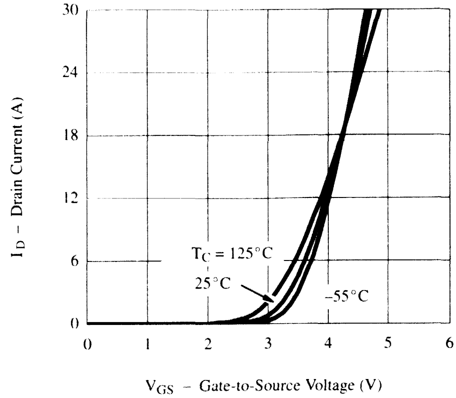


Typical Characteristics (25 °C Unless Noted) N-Channel 2

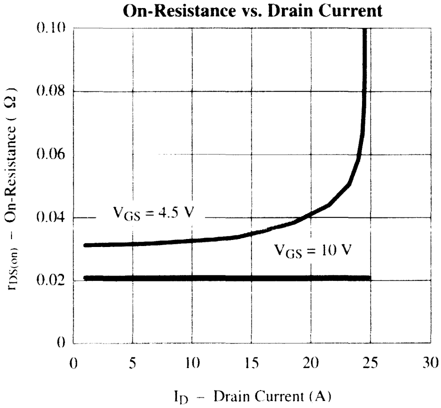
Output Characteristics



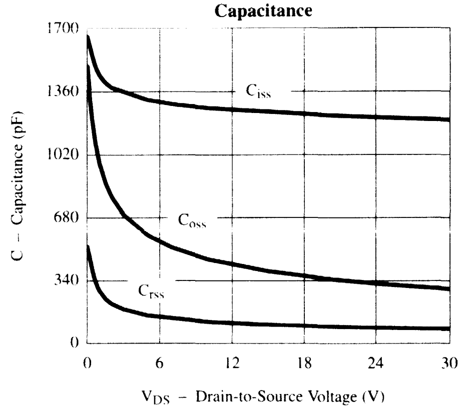
Transfer Characteristics



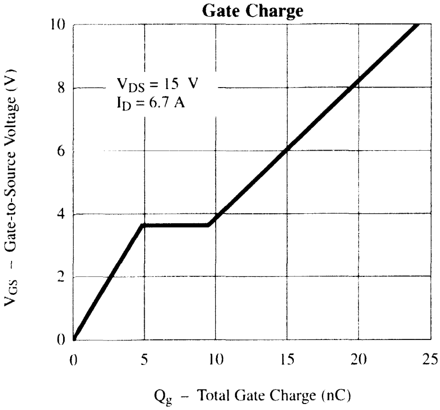
On-Resistance vs. Drain Current



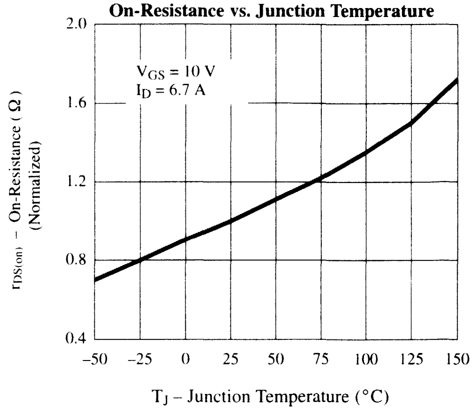
Capacitance



Gate Charge



On-Resistance vs. Junction Temperature



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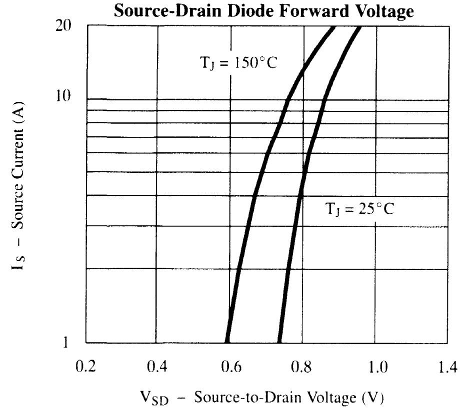
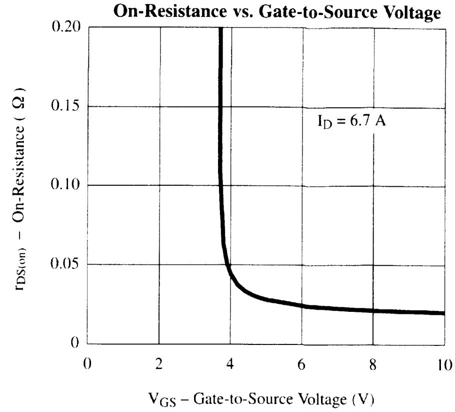
Typical Characteristics (25°C Unless Noted)

N-Channel 2

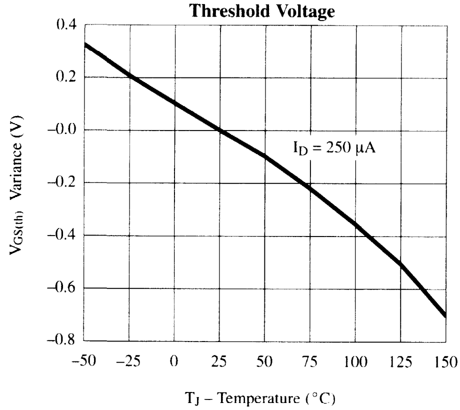
Source-Drain Diode Forward Voltage



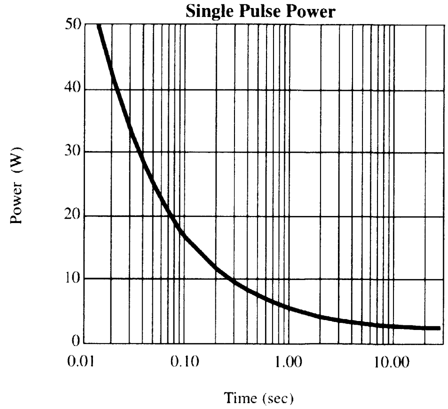
On-Resistance vs. Gate-to-Source Voltage



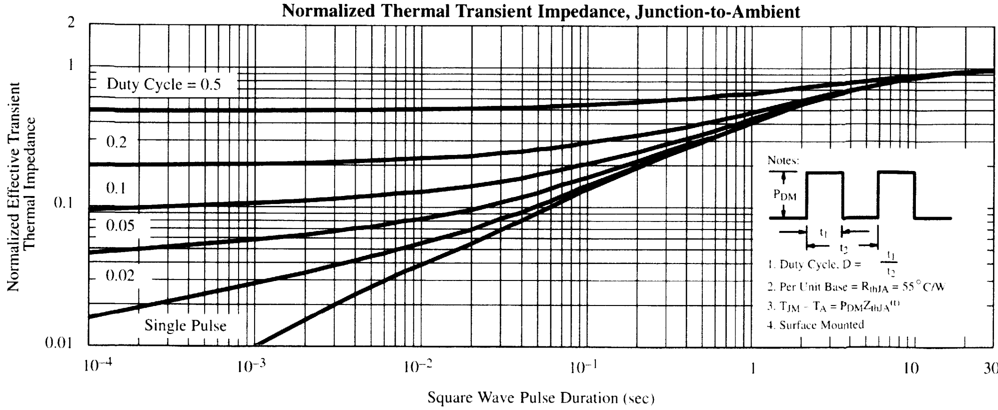
Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient



New Product

TEMIC
Semiconductors

Si4925DY

Dual P-Channel 30-V (D-S) Rated MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
–30	0.032 @ V_{GS} = –10 V	± 6.1
	0.045 @ V_{GS} = –4.5 V	± 5.1

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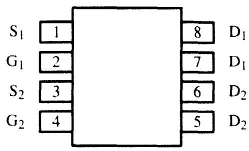
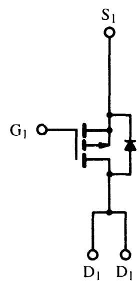
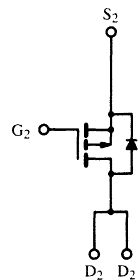


Top View



P-Channel MOSFET



P-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	–30	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	± 6.1	A
	T_A = 70°C		± 4.9	
Pulsed Drain Current		I_{DM}	± 40	
Continuous Source Current (Diode Conduction)[a]		I_S	–1.7	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	2.0	W
	T_A = 70°C		1.3	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient[a]	R_{thJA}	62.5	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70642. A SPICE Model data sheet is available for this product (FaxBack document #70635).

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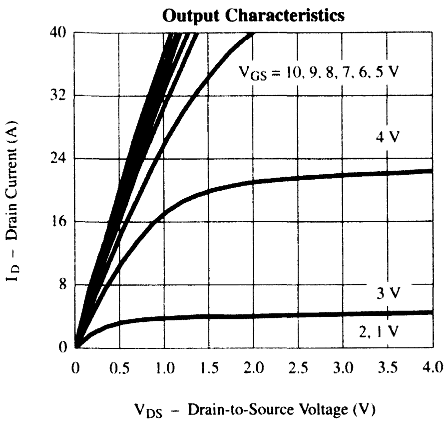
New Product

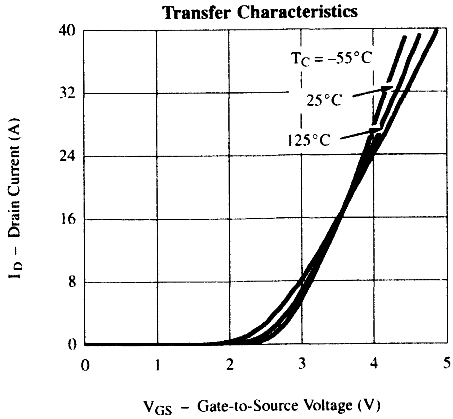
Specifications (T_J = 25°C Unless Otherwise Noted)

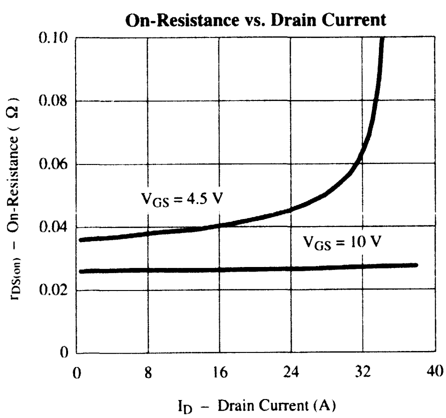
Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250\ \mu A$	−1			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = \pm 20$ V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -30$ V, $V_{GS} = 0$ V			−1	µA
		$V_{DS} = -30$ V, $V_{GS} = 0$ V, $T_J = 55°C$			−25	
On-State Drain Current[b]	$I_{D(on)}$	$V_{DS} \leq -5$ V, $V_{GS} = -10$ V	20			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	$V_{GS} = -10$ V, $I_D = -6.1$ A		0.026	0.032	Ω
		$V_{GS} = -4.5$ V, $I_D = -5.1$ A		0.036	0.045	
Forward Transconductance[b]	g_{fs}	$V_{DS} = -15$ V, $I_D = -6.1$ A		16		S
Diode Forward Voltage[b]	V_{SD}	$I_S = -1.7$ A, $V_{GS} = 0$ V			−1.2	V
Dynamic[a]						
Total Gate Charge	Q_g	$V_{DS} = -15$ V, $V_{GS} = -10$ V, $I_D = -6.1$ A		32.0	50	nC
Gate-Source Charge	Q_{gs}			7.0		
Gate-Drain Charge	Q_{gd}			5.0		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -15$ V, $R_L = 15\ \Omega$ $I_D \cong -1$ A, $V_{GEN} = -10$ V, $R_G = 6\ \Omega$		10	20	ns
Rise Time	t_r			10	20	
Turn-Off Delay Time	$t_{d(off)}$			55	80	
Fall Time	t_f			25	40	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -1.7$ A, di/dt = 100 A/µs		50	90	

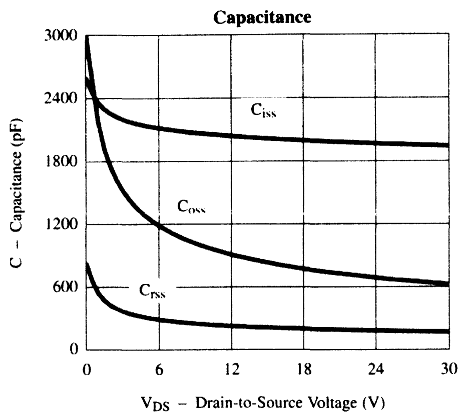
Notes
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

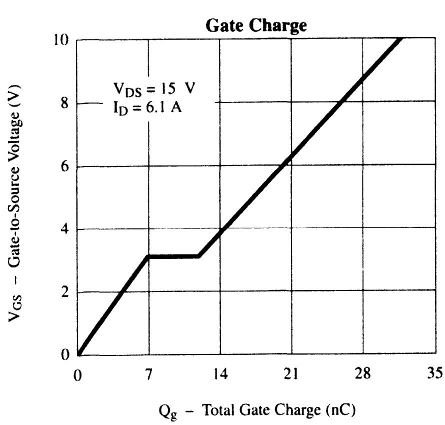
Typical Characteristics (25°C Unless Noted)

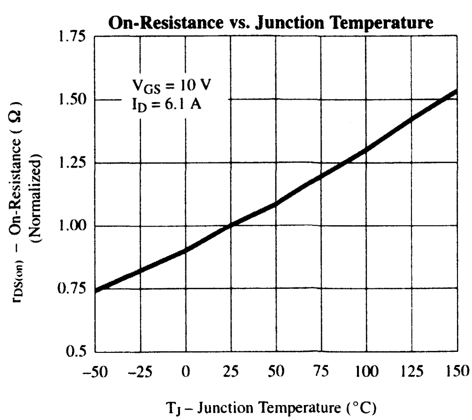








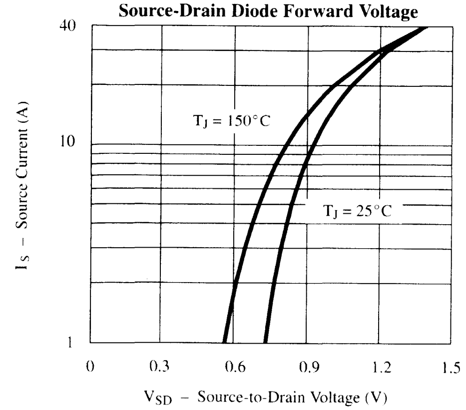




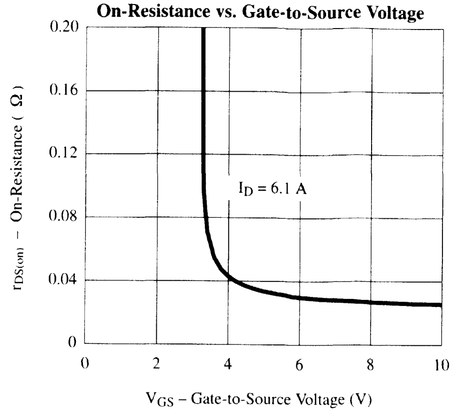
New Product

Typical Characteristics (25 °C Unless Noted)

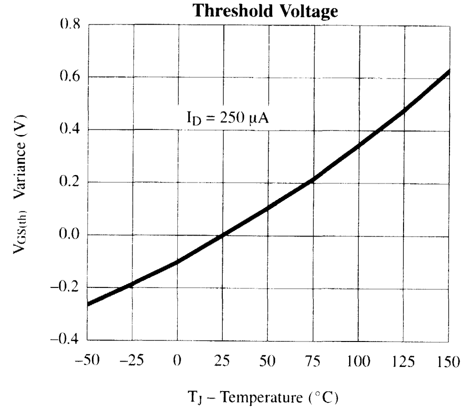
Source-Drain Diode Forward Voltage



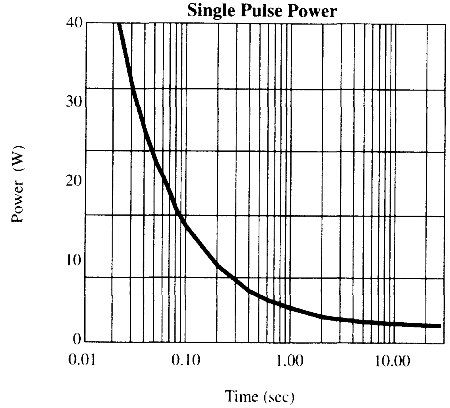
On-Resistance vs. Gate-to-Source Voltage



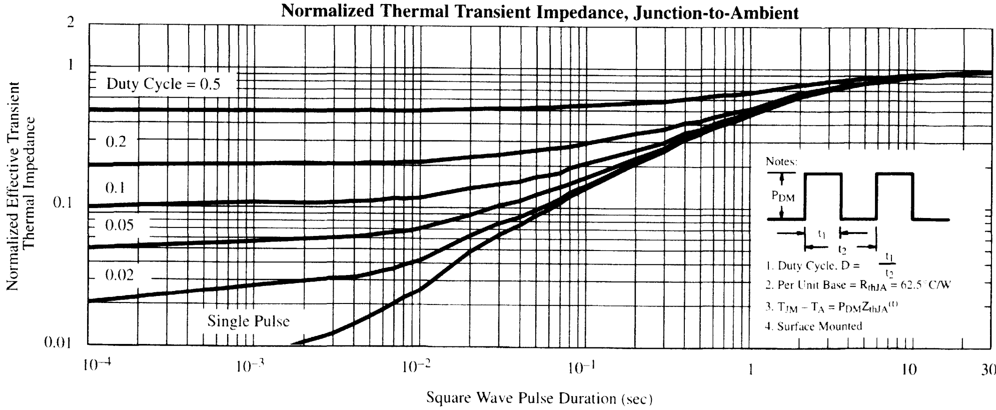
Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient



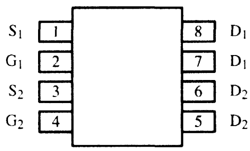
New Product

Dual N-Channel Enhancement-Mode MOSFET

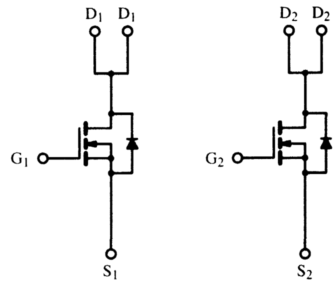
Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
30	0.037 @ V_{GS} = 10 V	±5.8
	0.055 @ V_{GS} = 4.5 V	±4.7

SO-8



Top View



N-Channel MOSFET N-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	±5.8	A
	T_A = 70°C		±4.6	
Pulsed Drain Current (10 µs Pulse Width)		I_{DM}	±30	
Continuous Source Current (Diode Conduction)[a]		I_S	1.7	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	2	W
	T_A = 70°C		1.3	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient[a]	R_{thJA}	62.5	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 10 sec.

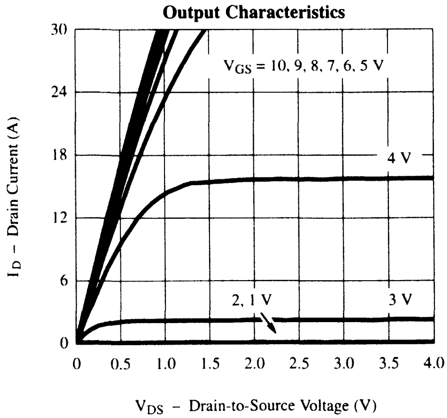
Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70150.
A SPICE Model data sheet is available for this product (FaxBack document #70556).

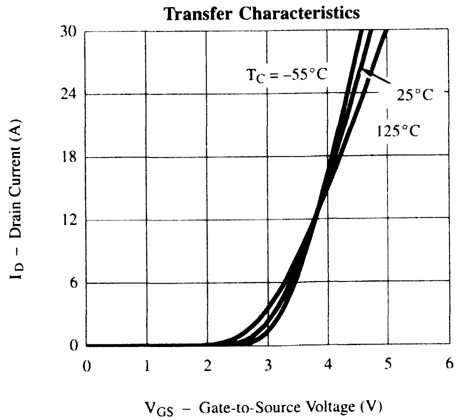
Specifications (T_J = 25°C Unless Otherwise Noted)

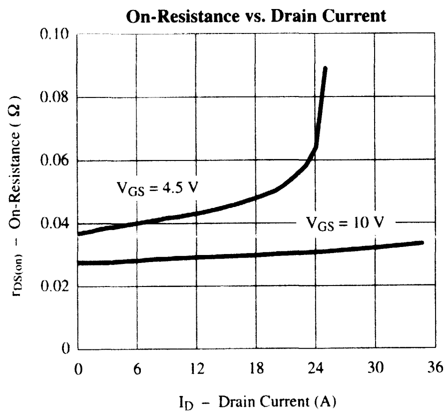
Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 µA	1			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V			1	µA
		V_{DS} = 30 V, V_{GS} = 0 V, T_J = 55°C			25	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 10 V	20			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 5.8 A		0.030	0.037	Ω
		V_{GS} = 4.5 V, I_D = 4.7 A		0.042	0.055	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 5.8 A		13		S
Diode Forward Voltage[b]	V_{SD}	I_S = 1.7 A, V_{GS} = 0 V		0.8	1.2	V
Dynamic[a]						
Total Gate Charge	Q_g	V_{DS} = 15 V, V_{GS} = 10 V, I_D = 5.8 A		18	25	nC
Gate-Source Charge	Q_{gs}			4.5		
Gate-Drain Charge	Q_{gd}			2.5		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 15 V, R_L = 15 Ω I_D ≅ 1 A, V_{GEN} = 10 V, R_G = 6 Ω		10	16	ns
Rise Time	t_r			10	16	
Turn-Off Delay Time	$t_{d(off)}$			27	40	
Fall Time	t_f			24	35	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 1.7 A, di/dt = 100 A/µs		45	80	

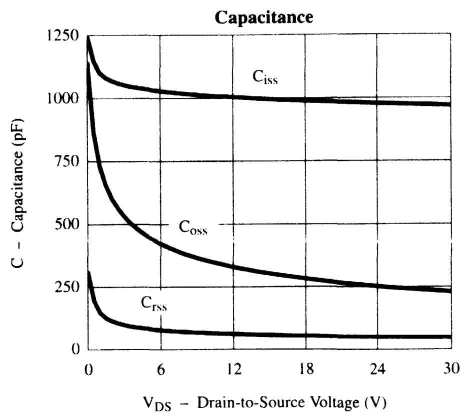
Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

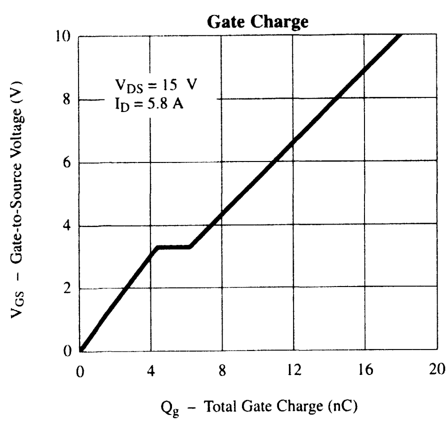
Typical Characteristics (25 °C Unless Otherwise Noted)

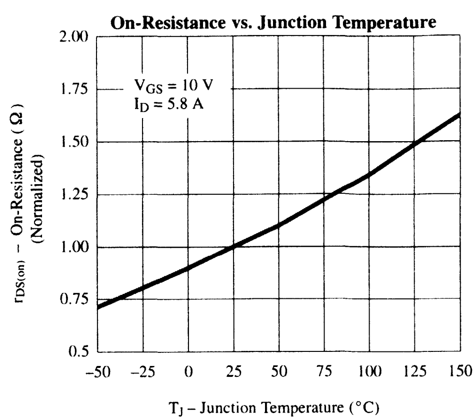






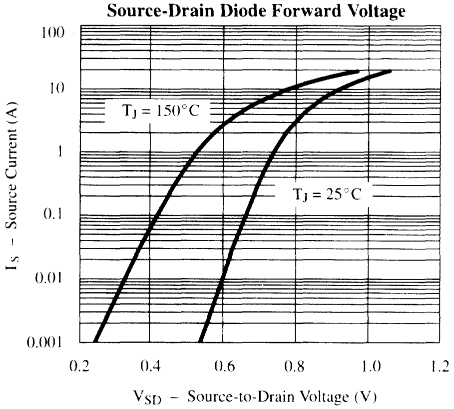




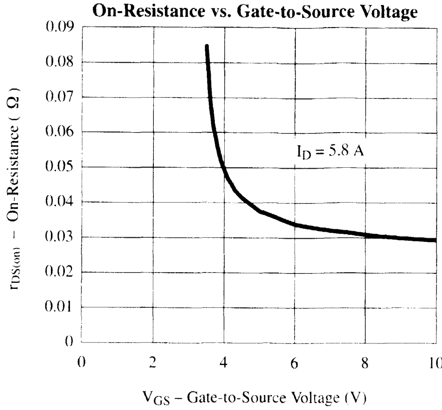


Typical Characteristics (25°C Unless Otherwise Noted)

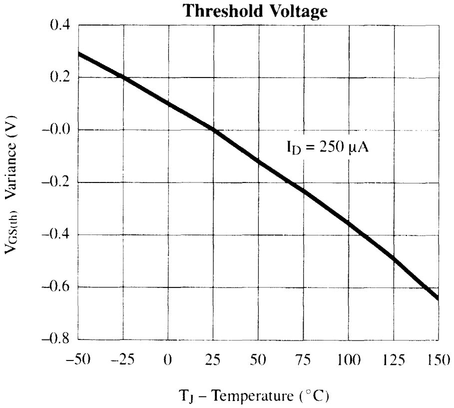
Source-Drain Diode Forward Voltage



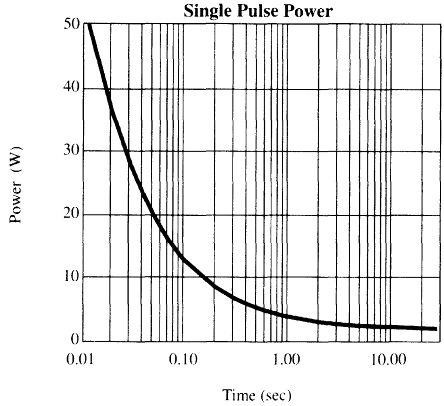
On-Resistance vs. Gate-to-Source Voltage



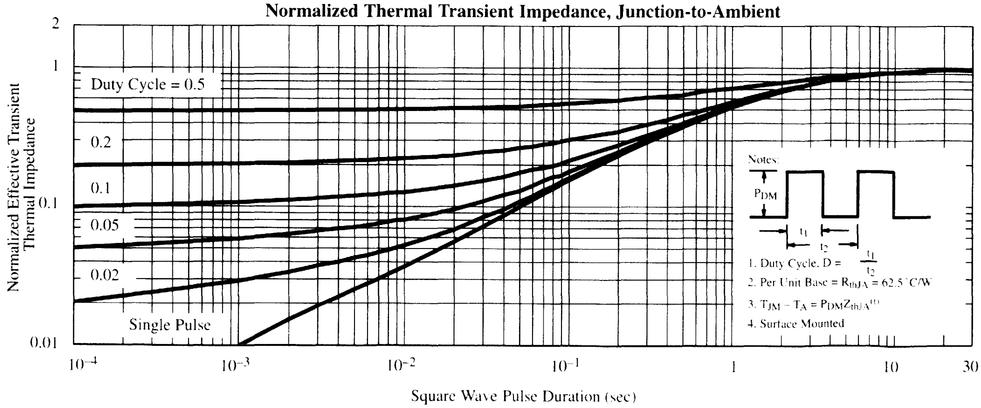
Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient



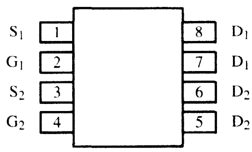
Dual N-Channel 60-V, 175°C Rated MOSFET

Product Summary

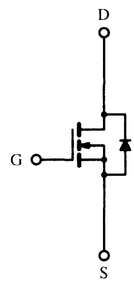
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
60	0.055 @ V_{GS} = 10 V	±4.5
	0.075 @ V_{GS} = 4.5 V	±3.9

175°C Rated
Maximum Junction Temperature
TrenchFET™
Power MOSFETS

SO-8



Top View



N-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current (T_J = 175°C)[a]	T_A = 25°C	I_D	±4.5	A
	T_A = 70°C		±3.8	
Pulsed Drain Current		I_{DM}	±30	A
Continuous Source Current (Diode Conduction)[a]		I_S	2	A
Maximum Power Dissipation[a]	T_A = 25°C	P_D	2.4	W
	T_A = 70°C		1.7	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 175	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient[a]	R_{thJA}	62.5	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70157.

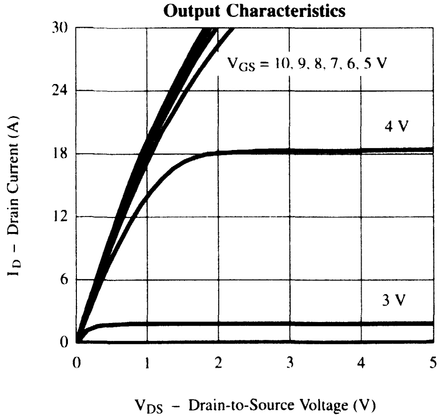
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 µA	1			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60 V, V_{GS} = 0 V			2	µA
		V_{DS} = 60 V, V_{GS} = 0 V, T_J = 55°C			25	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 10 V	20			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 4.5 A		0.045	0.055	Ω
		V_{GS} = 4.5 V, I_D = 3.9 A		0.055	0.075	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 4.5 A		13		S
Diode Forward Voltage[b]	V_{SD}	I_S = 2 A, V_{GS} = 0 V		0.9	1.2	V
Dynamic[a]						
Total Gate Charge	Q_g	V_{DS} = 30 V, V_{GS} = 10 V, I_D = 4.5 A		19	30	nC
Gate-Source Charge	Q_{gs}			4		
Gate-Drain Charge	Q_{gd}			3		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 30 V, R_L = 30 Ω I_D ≅ 1 A, V_{GEN} = 10 V, R_G = 6 Ω		13	20	ns
Rise Time	t_r			11	20	
Turn-Off Delay Time	$t_{d(off)}$			36	60	
Fall Time	t_f			11	20	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 2 A, di/dt = 100 A/µs		35	60	

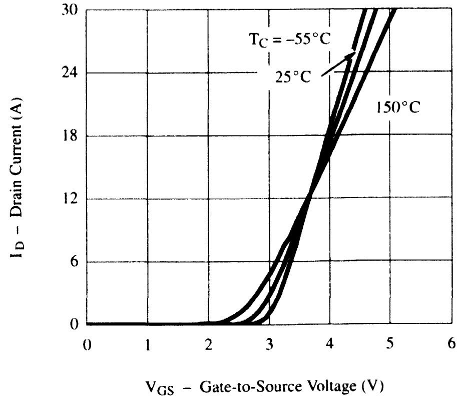
Notes
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

Typical Characteristics (25°C Unless Otherwise Noted)

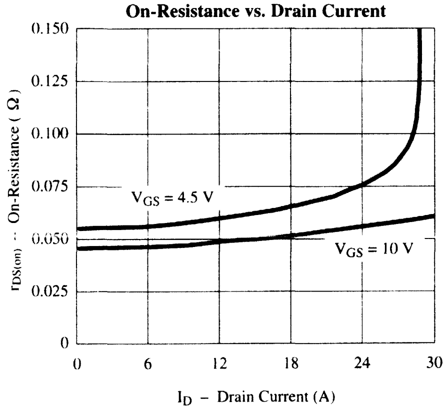
Output Characteristics



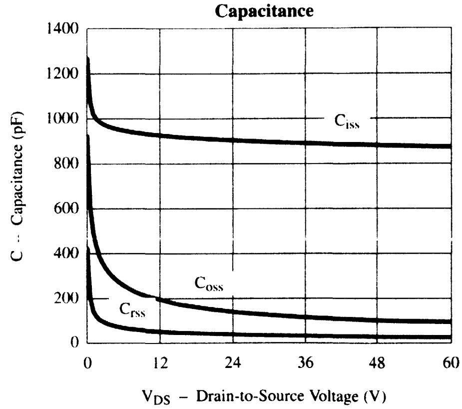
Transfer Characteristics



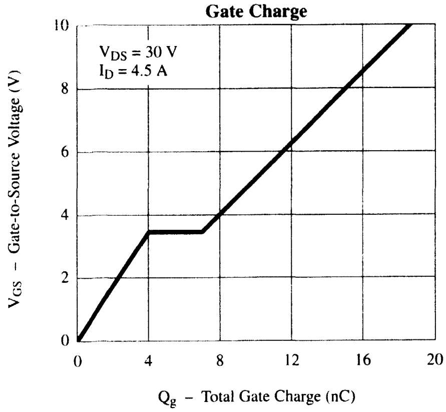
On-Resistance vs. Drain Current



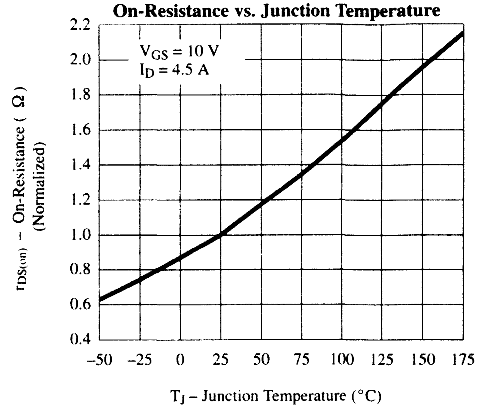
Capacitance



Gate Charge



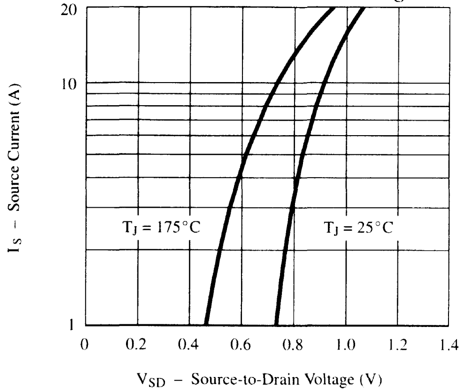
On-Resistance vs. Junction Temperature



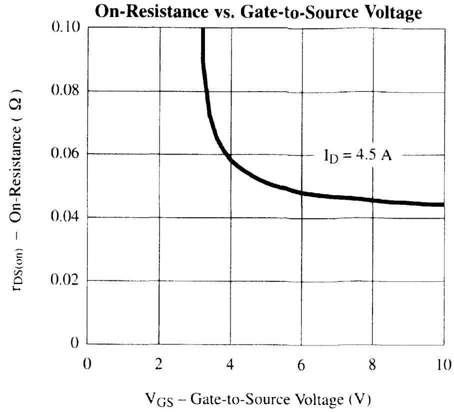
New Product

Typical Characteristics (25°C Unless Otherwise Noted)

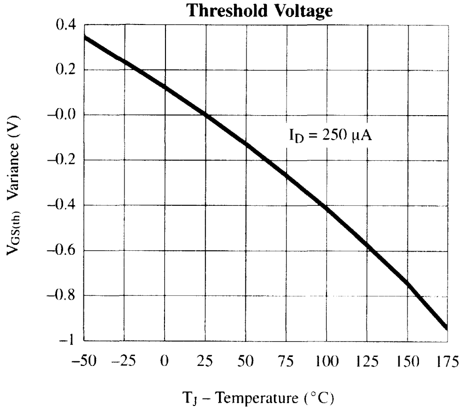
Source-Drain Diode Forward Voltage



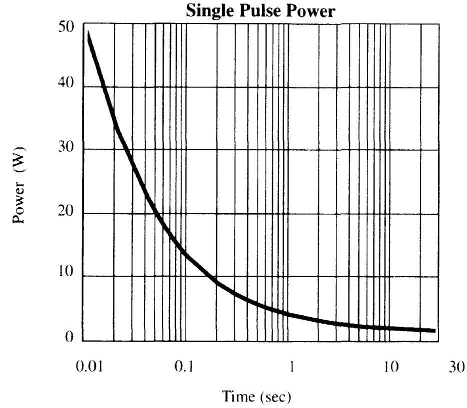
On-Resistance vs. Gate-to-Source Voltage



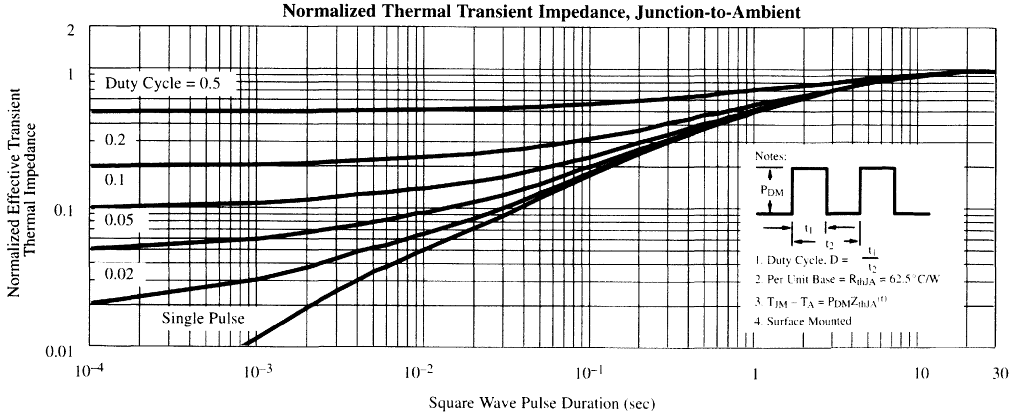
Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient



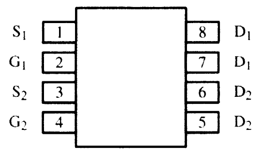
New Product

Dual P-Channel 30-V (D-S) Rated MOSFET

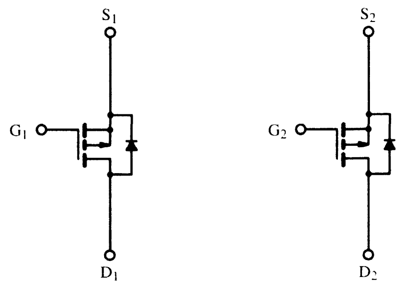
Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
–30	0.085 @ V_{GS} = –10 V	± 3.5
	0.19 @ V_{GS} = –4.5 V	± 2.5

SO-8



Top View



P-Channel MOSFET P-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	–30	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	± 3.5	A
	T_A = 70°C		± 2.8	
Pulsed Drain Current		I_{DM}	± 20	
Continuous Source Current (Diode Conduction)[a]		I_S	–1.7	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	2.0	W
	T_A = 70°C		1.3	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient[a]	R_{thJA}	62.5	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70156.
A SPICE Model data sheet is available for this product (FaxBack document #70554).

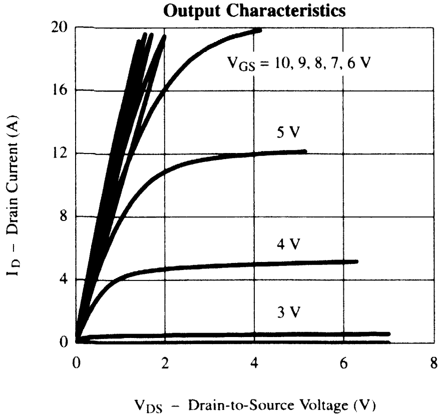
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250\ \mu A$	1.0			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = \pm 20$ V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -30$ V, $V_{GS} = 0$ V			–1	µA
		$V_{DS} = -30$ V, $V_{GS} = 0$ V, $T_J = 55°C$			–25	
On-State Drain Current[b]	$I_{D(on)}$	$V_{DS} \geq -5$ V, $V_{GS} = -10$ V	–15			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	$V_{GS} = -10$ V, $I_D = 2.5$ A		0.066	0.085	Ω
		$V_{GS} = -4.5$ V, $I_D = 1.8$ A		0.125	0.19	
Forward Transconductance[b]	g_{fs}	$V_{DS} = -15$ V, $I_D = -2.5$ A		5.0		S
Diode Forward Voltage[b]	V_{SD}	$I_S = -1.7$ A, $V_{GS} = 0$ V		–0.8	–1.2	V
Dynamic[a]						
Total Gate Charge	Q_g	$V_{DS} = -10$ V, $V_{GS} = -10$ V, $I_D = -2.5$ A		8.7	15	nC
Gate-Source Charge	Q_{gs}			1.9		
Gate-Drain Charge	Q_{gd}			1.3		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10$ V, $R_L = 10\ \Omega$, $I_D \cong -1$ A, $V_{GEN} = -10$ V, $R_G = 6\ \Omega$		7	15	ns
Rise Time	t_r			9	18	
Turn-Off Delay Time	$t_{d(off)}$			14	27	
Fall Time	t_f			8	15	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -1.7$ A, di/dt = 100 A/µs		50	80	

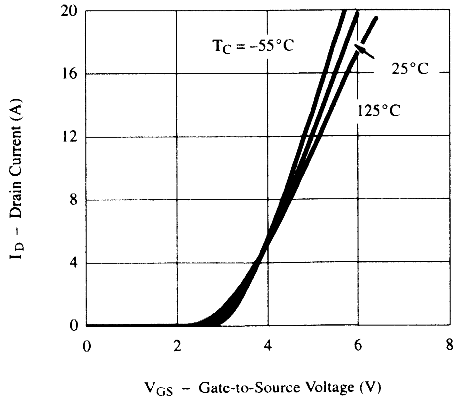
Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

Typical Characteristics (25°C Unless Otherwise Noted)

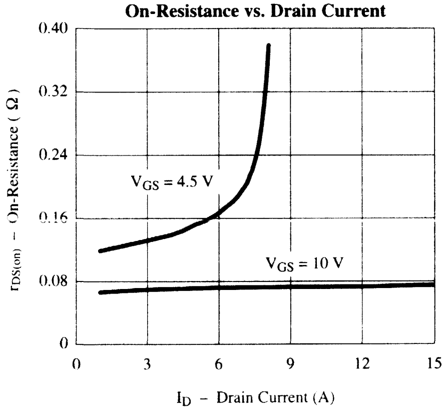
Output Characteristics



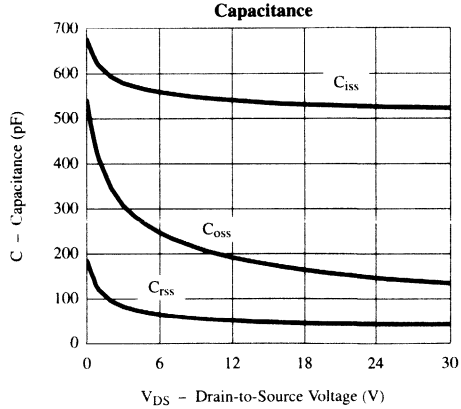
Transfer Characteristics



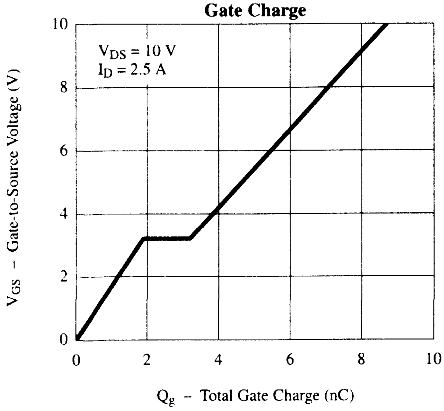
On-Resistance vs. Drain Current



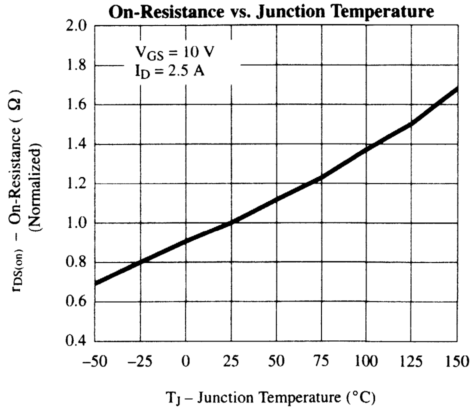
Capacitance



Gate Charge

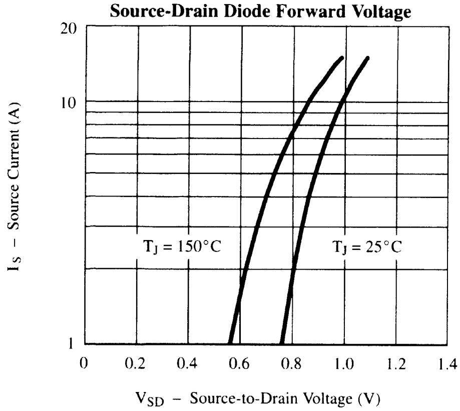


On-Resistance vs. Junction Temperature

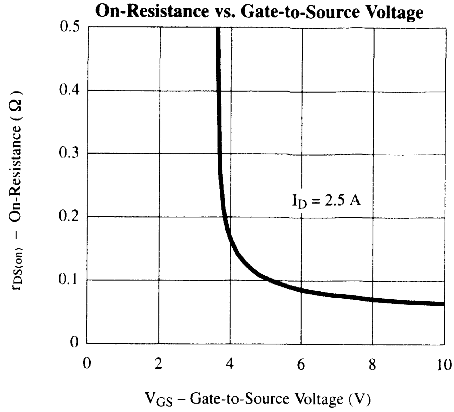


Typical Characteristics (25° C Unless Otherwise Noted)

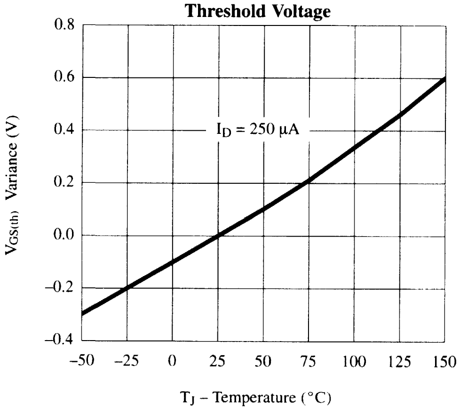
Source-Drain Diode Forward Voltage



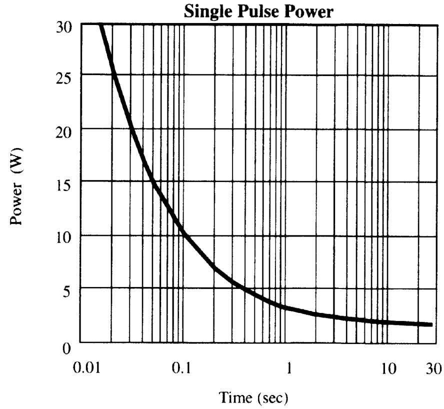
On-Resistance vs. Gate-to-Source Voltage



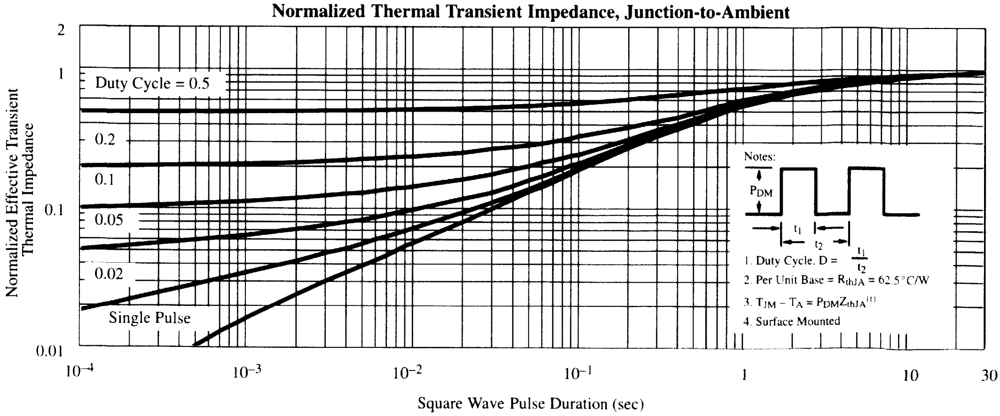
Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient



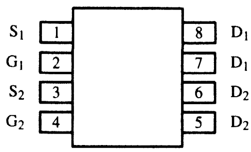
Dual P-Channel 60-V, 175°C Rated MOSFET

Product Summary

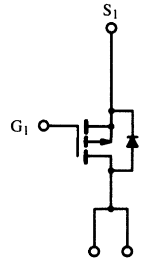
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
–60	0.120 @ V_{GS} = –10 V	± 3.1
	0.150 @ V_{GS} = –4.5 V	± 2.8

175°C Rated
Maximum Junction Temperature
TrenchFET™
Power MOSFETs

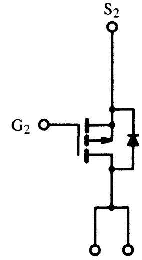
SO-8



Top View



P-Channel MOSFET



P-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	–60	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 175°C)[a]	T_A = 25°C	I_D	± 3.1	A
	T_A = 70°C		± 2.6	
Pulsed Drain Current		I_{DM}	± 30	
Continuous Source Current (Diode Conduction)[a]		I_S	–2.0	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	2.4	W
	T_A = 70°C		1.7	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 175	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient[a]	R_{thJA}	62.5	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70166.

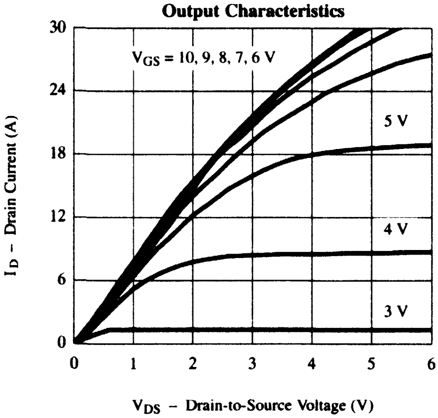
Specifications (T_J = 25 °C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250$ µA	–1			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = \pm 20$ V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -60$ V, $V_{GS} = 0$ V			–2	µA
		$V_{DS} = -60$ V, $V_{GS} = 0$ V, $T_J = 55$°C			–25	
On-State Drain Current[b]	$I_{D(on)}$	$V_{DS} \leq -5$ V, $V_{GS} = -10$ V	–20			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	$V_{GS} = -10$ V, $I_D = -3.1$ A		0.100	0.120	Ω
		$V_{GS} = -4.5$ V, $I_D = -2.8$ A		0.125	0.150	
Forward Transconductance[b]	g_{fs}	$V_{DS} = -15$ V, $I_D = -3.1$ A		7.5		S
Diode Forward Voltage[b]	V_{SD}	$I_S = -2.0$ A, $V_{GS} = 0$ V		–0.8	–1.2	V
Dynamic[a]						
Total Gate Charge	Q_g	$V_{DS} = -30$ V, $V_{GS} = -10$ V, $I_D = -3.1$ A		16	25	nC
Gate-Source Charge	Q_{gs}			4		
Gate-Drain Charge	Q_{gd}			1.6		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -30$ V, $R_L = 30$ Ω $I_D \cong -1$ A, $V_{GEN} = -10$ V, $R_G = 6$ Ω		8	15	ns
Rise Time	t_r			10	20	
Turn-Off Delay Time	$t_{d(off)}$			12	25	
Fall Time	t_f			35	50	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -2.0$ A, di/dt = 100 A/µs		60	90	

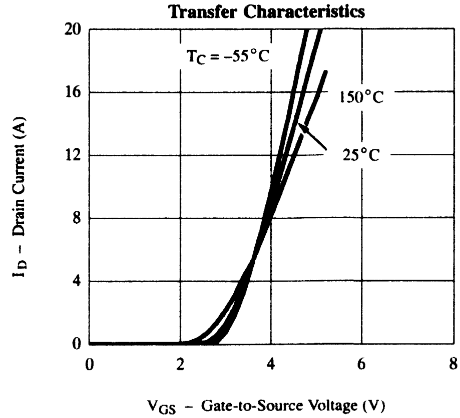
Notes
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

Typical Characteristics (25°C Unless Noted)

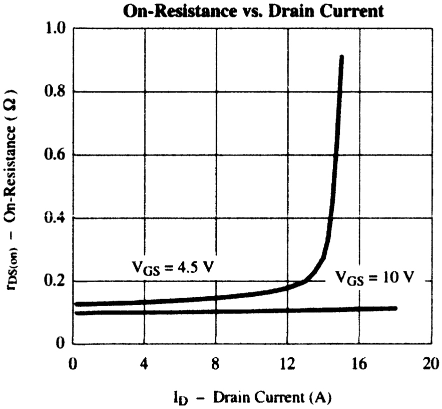
Output Characteristics



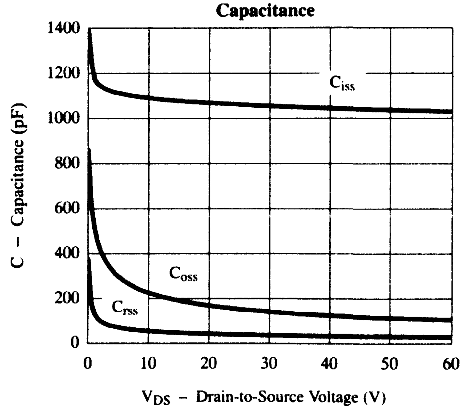
Transfer Characteristics



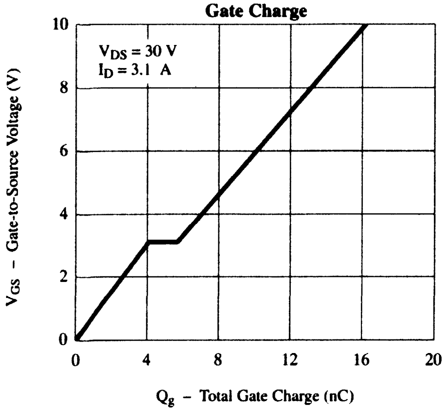
On-Resistance vs. Drain Current



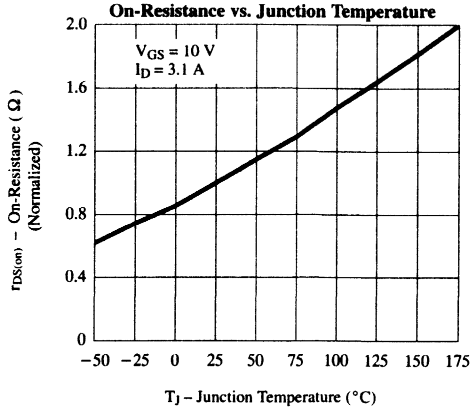
Capacitance



Gate Charge

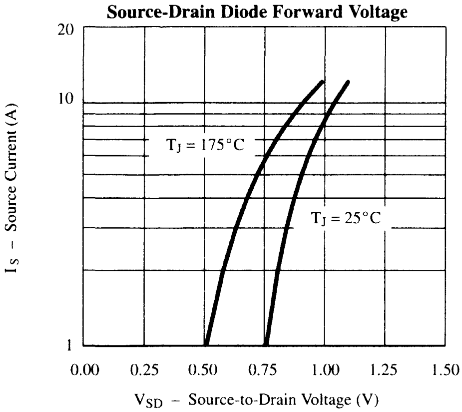


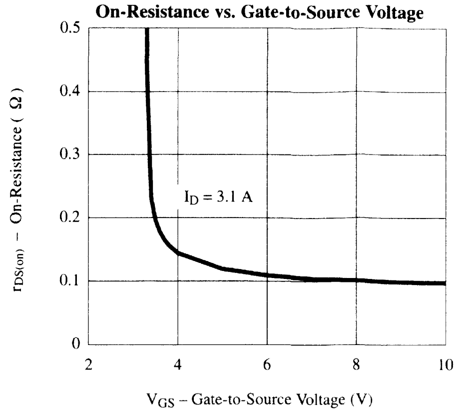
On-Resistance vs. Junction Temperature

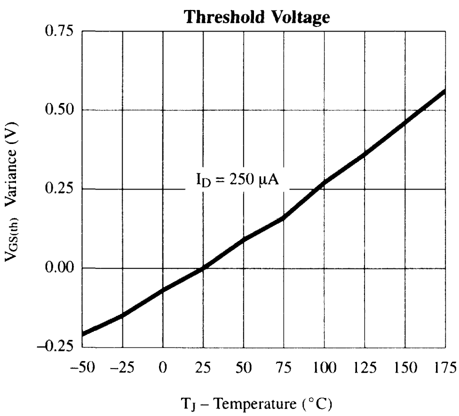


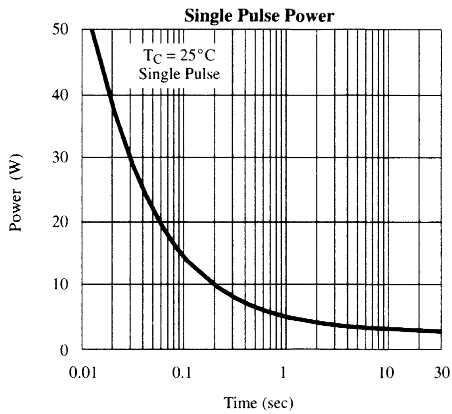
New Product

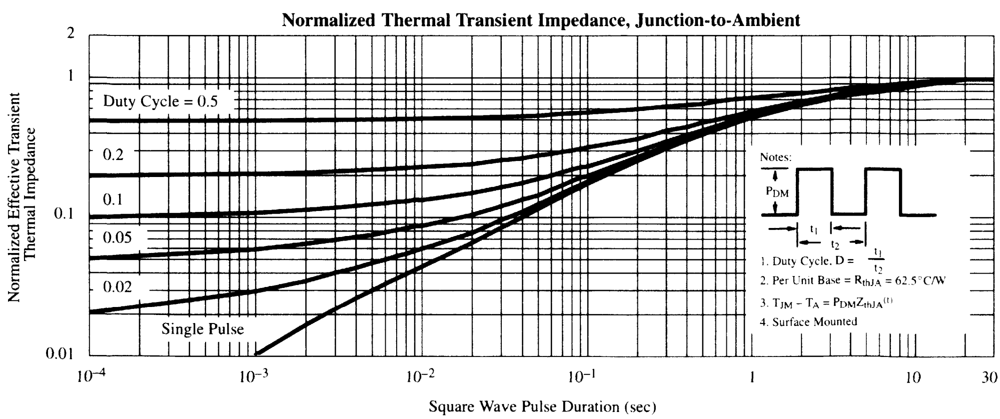
Typical Characteristics (25°C Unless Noted)











TEMIC
Semiconductors

Si4953DY

Dual P-Channel Enhancement-Mode MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
–30	0.053 @ V_{GS} = –10 V	±4.9
	0.095 @ V_{GS} = –4.5 V	±3.6

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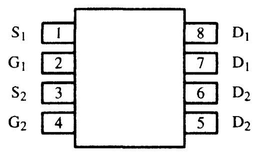
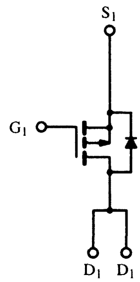
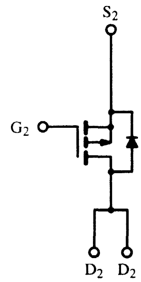


Top View



P-Channel MOSFET



P-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	–30	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	±4.9	A
	T_A = 70°C		±3.9	
Pulsed Drain Current		I_{DM}	±30	
Continuous Source Current (Diode Conduction)[a]		I_S	–1.7	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	2.0	W
	T_A = 70°C		1.3	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient[a]	R_{thJA}	62.5	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 10 sec.

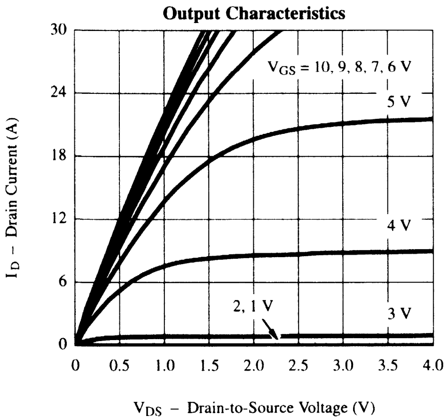
Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70153. A SPICE Model data sheet is available for this product (FaxBack document #70557).

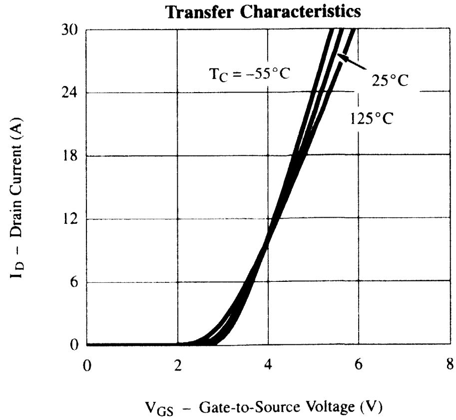
Specifications ($T_J = 25°C$ Unless Otherwise Noted)

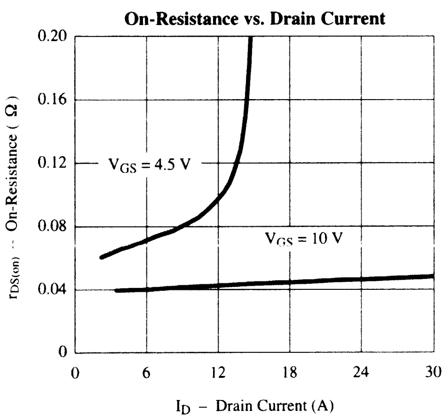
Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250\ \mu A$	–1			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ V$, $V_{GS} = \pm 20\ V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -30\ V$, $V_{GS} = 0\ V$			–1	µA
		$V_{DS} = -30\ V$, $V_{GS} = 0\ V$, $T_J = 55°C$			–25	
On-State Drain Current[b]	$I_{D(on)}$	$V_{DS} \leq -5\ V$, $V_{GS} = -10\ V$	–20			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	$V_{GS} = -10\ V$, $I_D = -4.9\ A$		0.043	0.053	Ω
		$V_{GS} = -4.5\ V$, $I_D = -3.6\ A$		0.070	0.095	
Forward Transconductance[b]	g_{fs}	$V_{DS} = -15\ V$, $I_D = -4.9\ A$		10		S
Diode Forward Voltage[b]	V_{SD}	$I_S = -1.7\ A$, $V_{GS} = 0\ V$		0.8	–1.2	V
Dynamic[a]						
Total Gate Charge	Q_g	$V_{DS} = -15\ V$, $V_{GS} = -10\ V$, $I_D = -4.9\ A$		16	25	nC
Gate-Source Charge	Q_{gs}			5		
Gate-Drain Charge	Q_{gd}			2		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -15\ V$, $R_L = 15\ \Omega$ $I_D \cong -1\ A$, $V_{GEN} = -10\ V$, $R_G = 6\ \Omega$		9	15	ns
Rise Time	t_r			13	20	
Turn-Off Delay Time	$t_{d(off)}$			25	40	
Fall Time	t_f			15	25	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -1.7\ A$, di/dt = 100 A/µs		60	90	

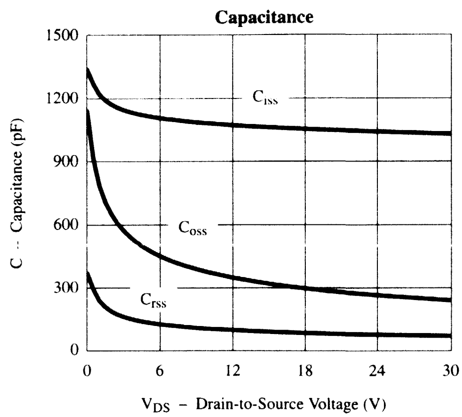
Notes
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

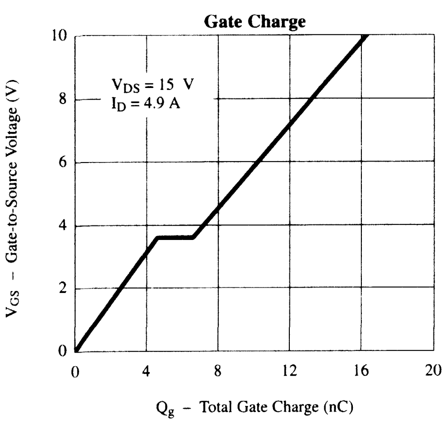
Typical Characteristics (25°C Unless Noted)

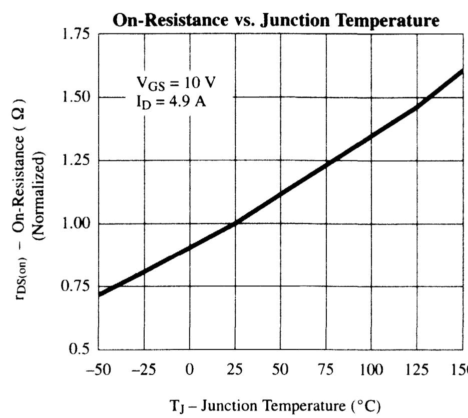






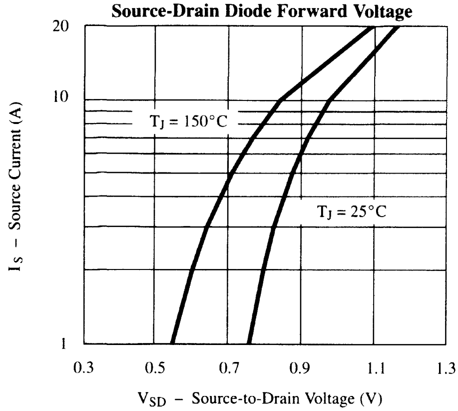




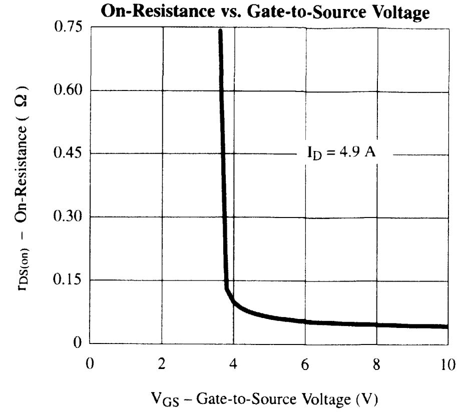


Typical Characteristics (25 °C Unless Noted)

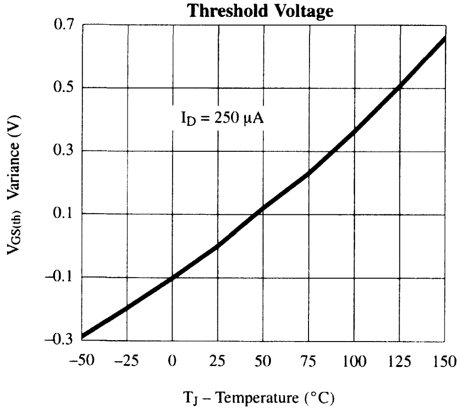
Source-Drain Diode Forward Voltage



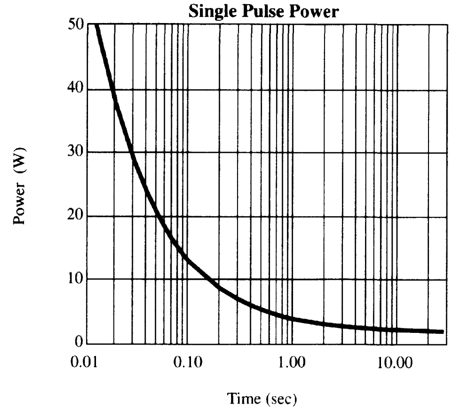
On-Resistance vs. Gate-to-Source Voltage



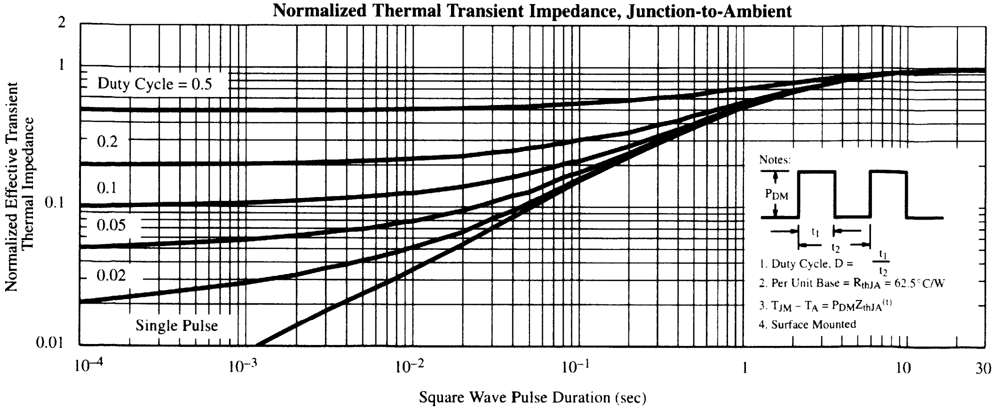
Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient



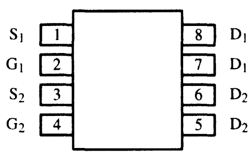
Dual N-Channel 80-V Rated MOSFET

Product Summary

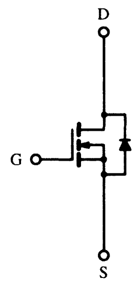
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
80	0.075 @ V_{GS} = 10 V	± 3.7
	0.095 @ V_{GS} = 6.0 V	± 3.2

TrenchFET™ Power MOSFETs

SO-8



Top View



N-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	80	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	± 3.7	A
	T_A = 70°C		± 2.9	
Pulsed Drain Current		I_{DM}	± 30	
Continuous Source Current (Diode Conduction)[a]		I_S	1.7	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	2.0	W
	T_A = 70°C		1.3	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient[a]	R_{thJA}	62.5	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70646.

New Product

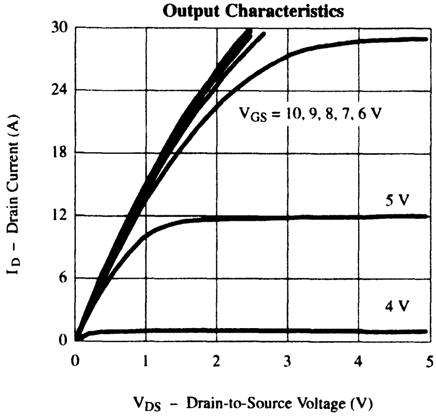
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 µA	2			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80 V, V_{GS} = 0 V			1	µA
		V_{DS} = 80 V, V_{GS} = 0 V, T_J = 55°C			20	
On-State Drain Curren[b]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 10 V	20			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 3.7 A		0.062	0.075	Ω
		V_{GS} = 6.0 V, I_D = 3.2 A		0.071	0.095	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 3.7 A		12		S
Diode Forward Voltage[b]	V_{SD}	I_S = 1.7 A, V_{GS} = 0 V			1.2	V
Dynamic[a]						
Total Gate Charge	Q_g	V_{DS} = 40 V, V_{GS} = 10 V, I_D = 3.7 A		15	30	nC
Gate-Source Charge	Q_{gs}			4		
Gate-Drain Charge	Q_{gd}			3.2		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 40 V, R_L = 40 Ω $I_D \cong$ 1 A, V_{GEN} = 10 V, R_G = 6 Ω		10	20	ns
Rise Time	t_r			10	20	
Turn-Off Delay Time	$t_{d(off)}$			30	30	
Fall Time	t_f			10	20	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 1.7 A, di/dt = 100 A/µs		75	110	

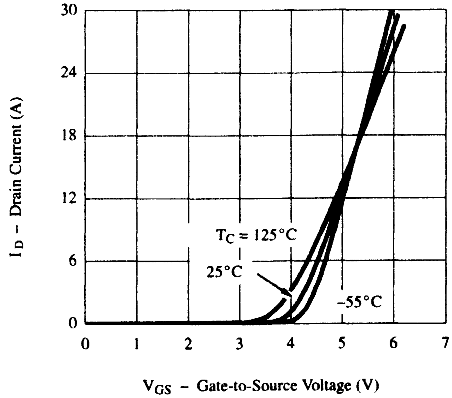
Notes
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

Typical Characteristics (25° C Unless Otherwise Noted)

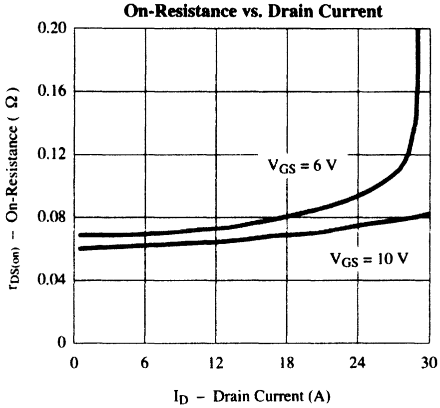
Output Characteristics



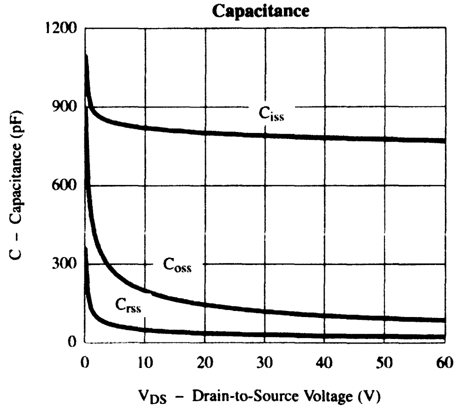
Transfer Characteristics



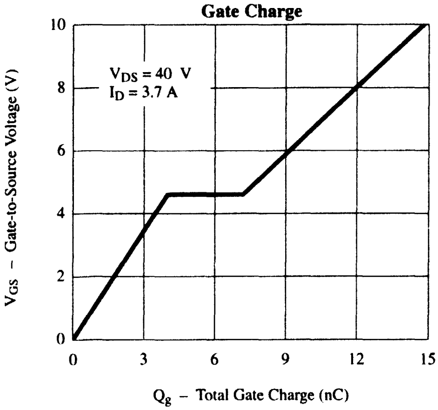
On-Resistance vs. Drain Current



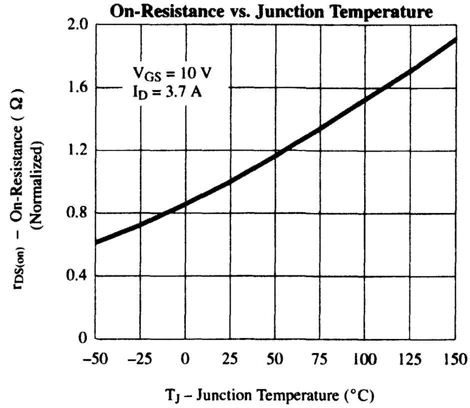
Capacitance



Gate Charge

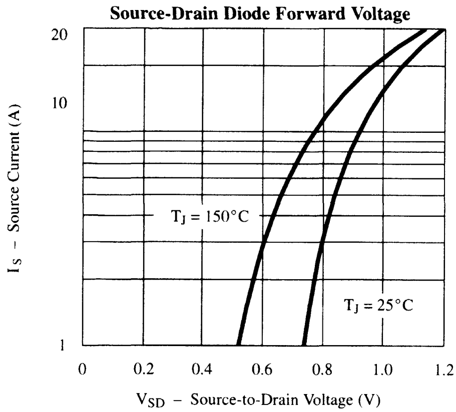


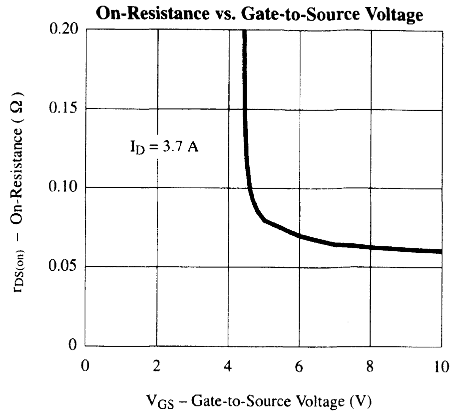
On-Resistance vs. Junction Temperature

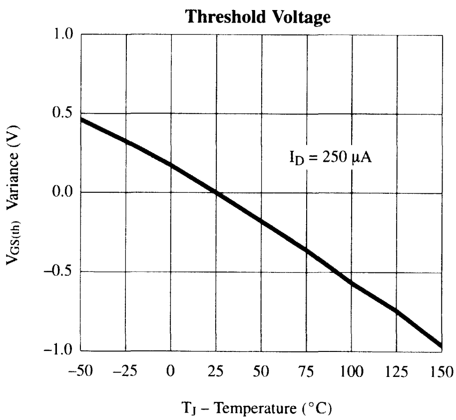


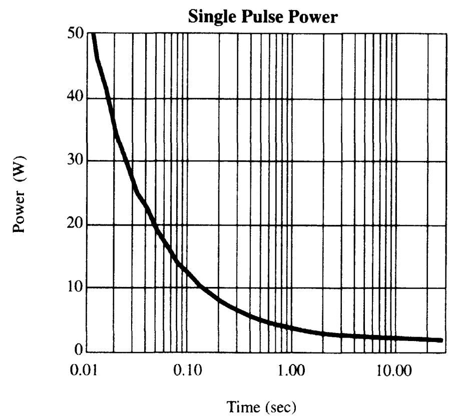
New Product

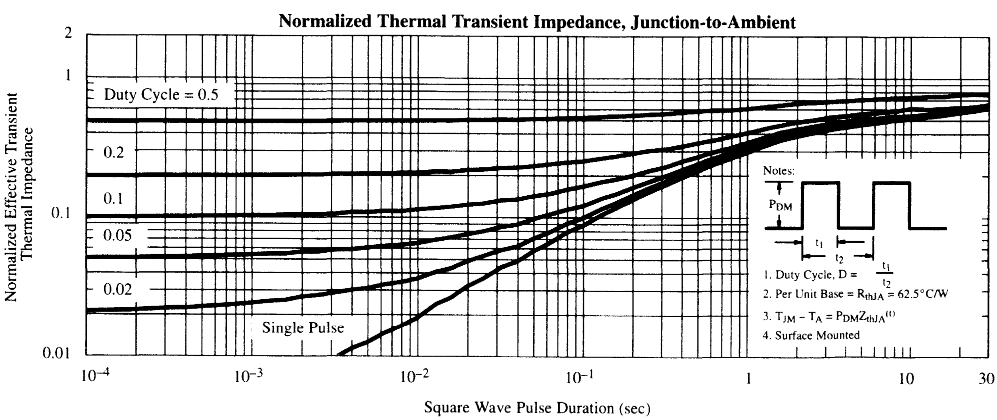
Typical Characteristics (25°C Unless Otherwise Noted)











New Product

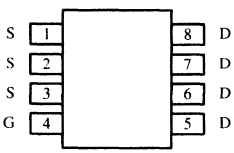
P-Channel 2.5-V (G-S) Rated MOSFET

Product Summary

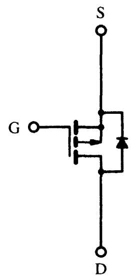
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
–12	0.025 @ V_{GS} = –4.5 V	± 7.7
	0.033 @ V_{GS} = –2.5 V	± 6.6

2.5-V Rated

SO-8



Top View



P-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	–12	V
Gate-Source Voltage		V_{GS}	± 8	
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	± 7.7	A
	T_A = 70°C		± 6.2	
Pulsed Drain Current		I_{DM}	± 30	
Continuous Source Current (Diode Conduction)[a]		I_S	–2.3	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	2.5	W
	T_A = 70°C		1.6	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient[a]	R_{thJA}	50	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70164.

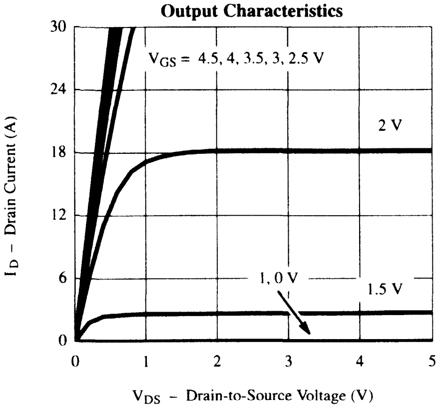
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250\ \mu A$	–0.6			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = \pm 8$ V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -12$ V, $V_{GS} = 0$ V			–1	µA
		$V_{DS} = -12$ V, $V_{GS} = 0$ V, $T_J = 55°C$			–5	
On-State Drain Current[b]	$I_{D(on)}$	$V_{DS} \leq -5$ V, $V_{GS} = -4.5$ V	–30			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	$V_{GS} = -4.5$ V, $I_D = -7.7$ A		0.019	0.025	Ω
		$V_{GS} = -2.5$ V, $I_D = -6.6$ A		0.024	0.033	
Forward Transconductance[b]	g_{fs}	$V_{DS} = -10$ V, $I_D = -7.7$ A		25		S
Diode Forward Voltage[b]	V_{SD}	$I_S = -2.3$ A, $V_{GS} = 0$ V		–0.72	–1.2	V
Dynamic[a]						
Total Gate Charge	Q_g	$V_{DS} = -6$ V, $V_{GS} = -4.5$ V, $I_D = -7.7$ A		46	80	nC
Gate-Source Charge	Q_{gs}			6		
Gate-Drain Charge	Q_{gd}			13		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -6$ V, $R_L = 6\ \Omega$ $I_D \cong -1$ A, $V_{GEN} = -4.5$ V, $R_G = 6\ \Omega$		40	80	ns
Rise Time	t_r			65	130	
Turn-Off Delay Time	$t_{d(off)}$			240	400	
Fall Time	t_f			140	250	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -2.3$ A, di/dt = 100 A/µs		70	120	

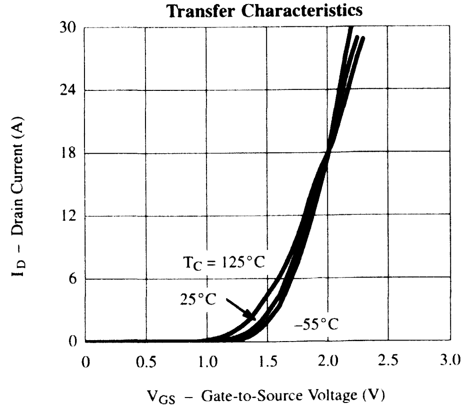
Notes
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

Typical Characteristics (25°C Unless Otherwise Noted)

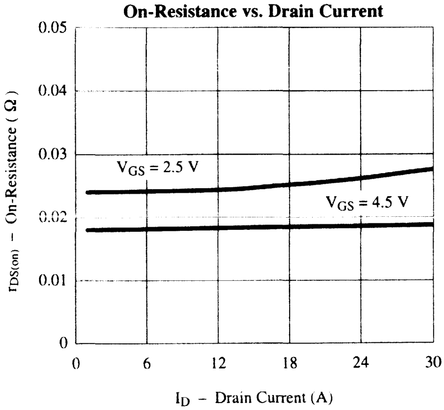
Output Characteristics



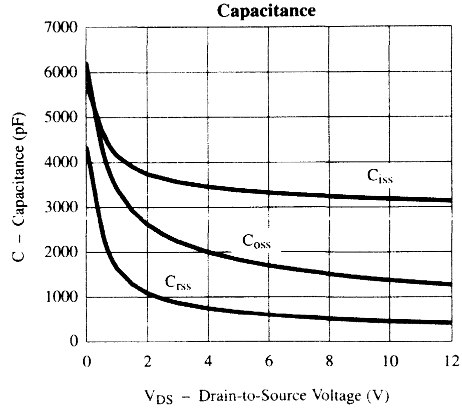
Transfer Characteristics



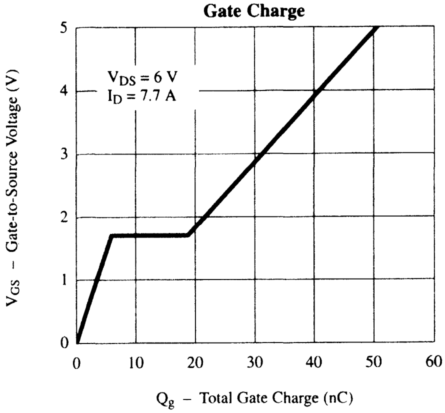
On-Resistance vs. Drain Current



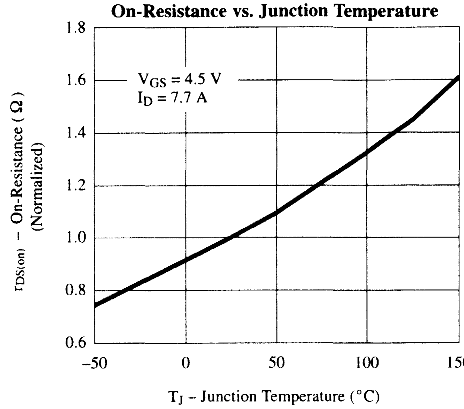
Capacitance



Gate Charge

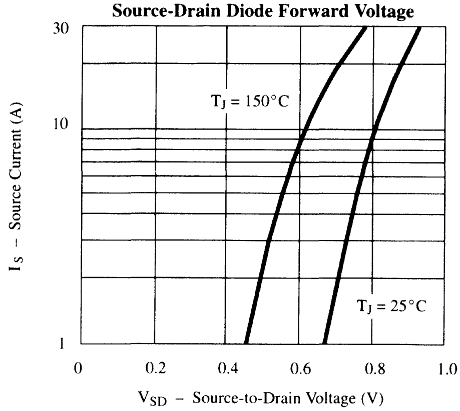


On-Resistance vs. Junction Temperature

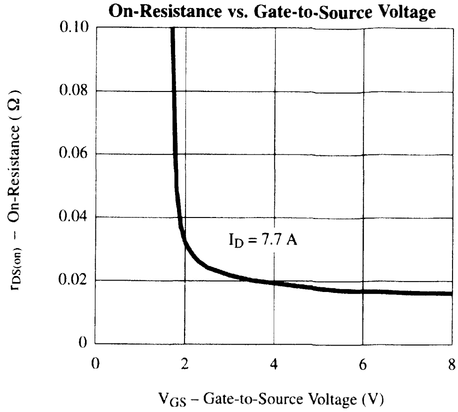


Typical Characteristics (25°C Unless Otherwise Noted)

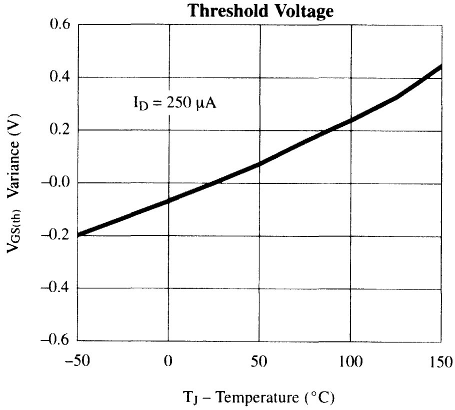
Source-Drain Diode Forward Voltage



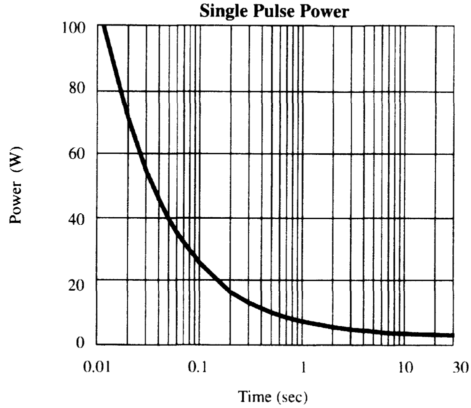
On-Resistance vs. Gate-to-Source Voltage



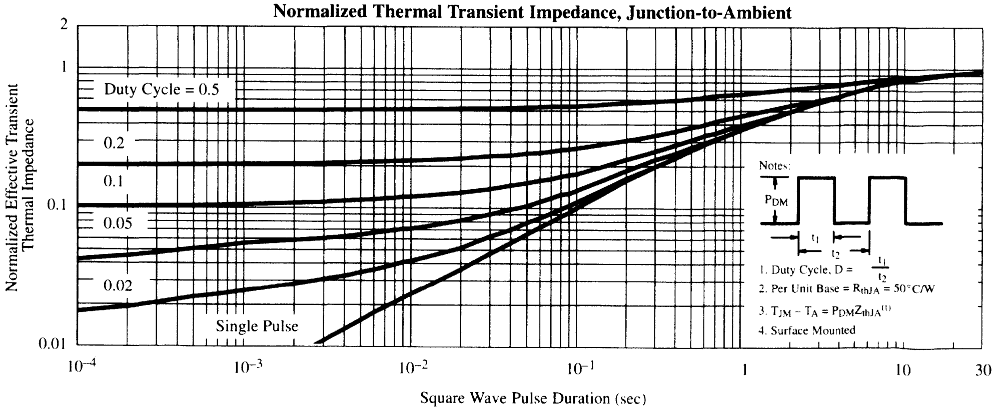
Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient



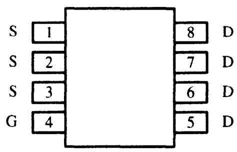
N-Channel 2.5-V (G-S) Rated MOSFET

Product Summary

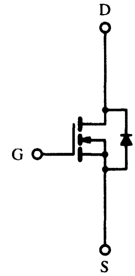
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
20	0.0135 @ V_{GS} = 4.5 V	± 10
	0.0160 @ V_{GS} = 2.5 V	± 9.3

2.5-V Rated

SO-8



Top View



N-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	± 8	
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	± 10	A
	T_A = 70°C		± 8	
Pulsed Drain Current (10 µs Pulse Width)		I_{DM}	± 30	
Continuous Source Current (Diode Conduction)[a]		I_S	2.3	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	2.5	W
	T_A = 70°C		1.6	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient[a]	R_{thJA}	50	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70160.

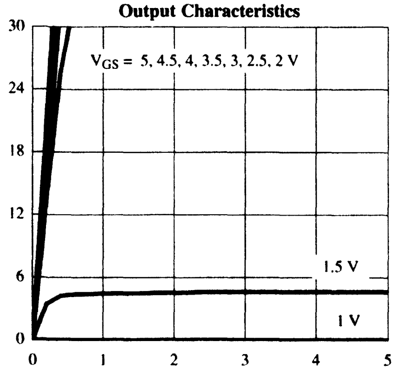
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\ \mu A$	0.6			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = \pm 8$ V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20$ V, $V_{GS} = 0$ V			1	µA
		$V_{DS} = 20$ V, $V_{GS} = 0$ V, $T_J = 55°C$			5	
On-State Drain Current[b]	$I_{D(on)}$	$V_{DS} \geq 5$ V, $V_{GS} = 4.5$ V	30			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	$V_{GS} = 4.5$ V, $I_D = 10$ A		0.0098	0.0135	Ω
		$V_{GS} = 2.5$ V, $I_D = 8$ A		0.011	0.0160	
Forward Transconductance[b]	g_{fs}	$V_{DS} = 10$ V, $I_D = 10$ A		57		S
Diode Forward Voltage[b]	V_{SD}	$I_S = 2.3$ A, $V_{GS} = 0$ V		0.71	1.2	V
Dynamic[a]						
Total Gate Charge	Q_g	$V_{DS} = 6$ V, $V_{GS} = 4.5$ V, $I_D = 10$ A		46.5	80	nC
Gate-Source Charge	Q_{gs}			5.5		
Gate-Drain Charge	Q_{gd}			13.5		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 6$ V, $R_L = 6\ \Omega$ $I_D \cong 1$ A, $V_{GEN} = 4.5$ V, $R_G = 6\ \Omega$		50	100	ns
Rise Time	t_r			110	200	
Turn-Off Delay Time	$t_{d(off)}$			150	300	
Fall Time	t_f			55	100	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 2.3$ A, di/dt = 100 A/µs		59	100	

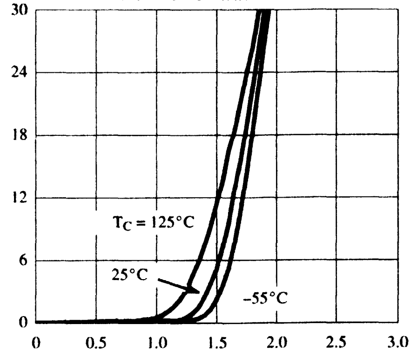
Notes
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

Typical Characteristics (25°C Unless Otherwise Noted)

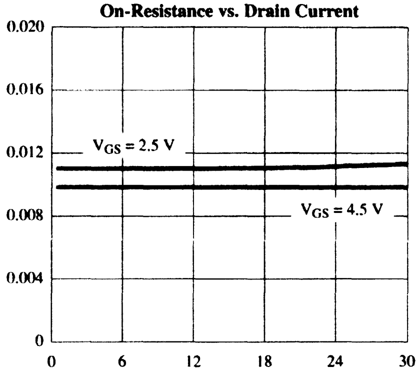
Output Characteristics



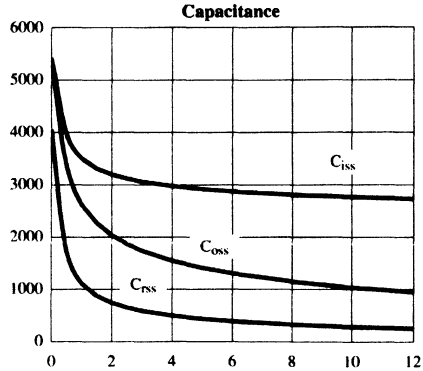
Transfer Characteristics



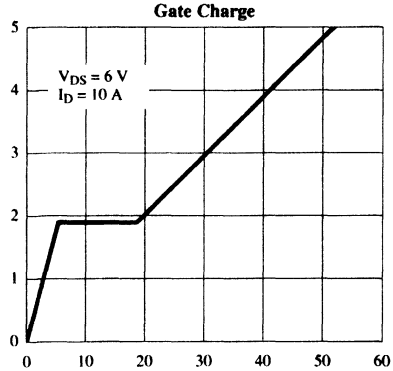
On-Resistance vs. Drain Current



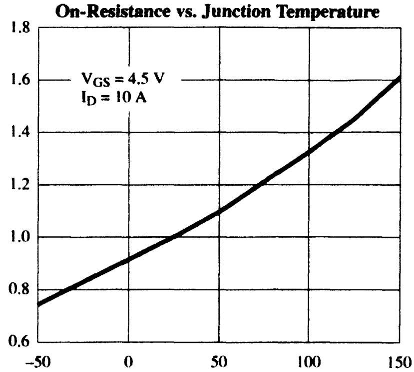
Capacitance



Gate Charge

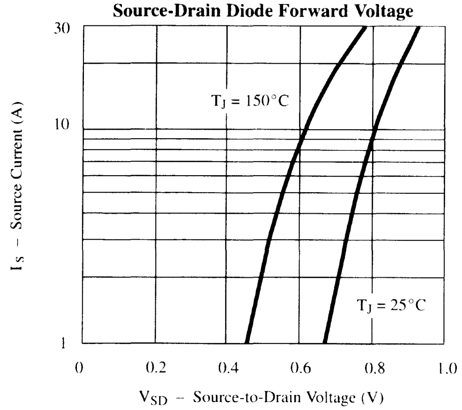


On-Resistance vs. Junction Temperature

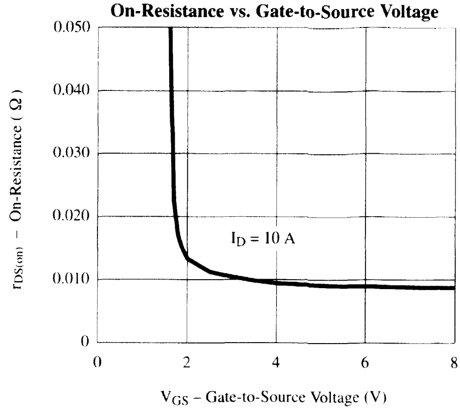


Typical Characteristics (25°C Unless Otherwise Noted)

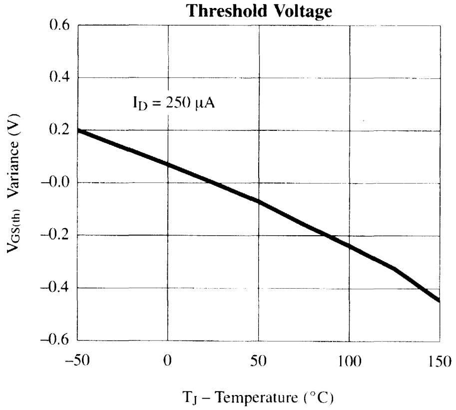
Source-Drain Diode Forward Voltage



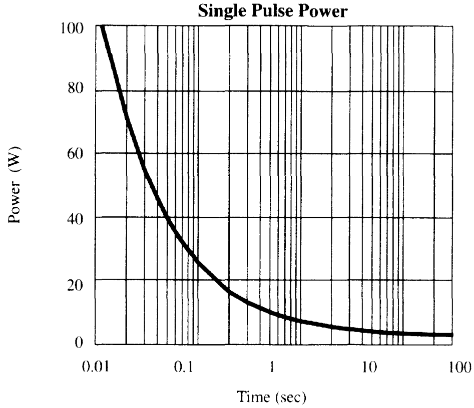
On-Resistance vs. Gate-to-Source Voltage



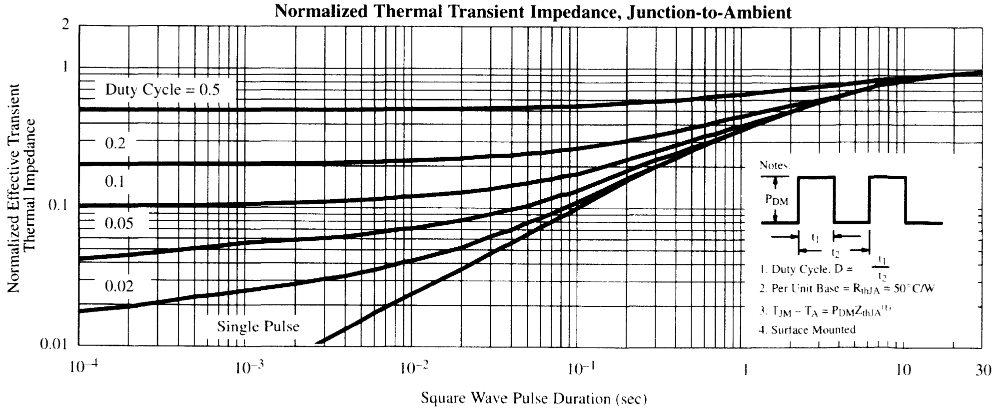
Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient



Si9529DY

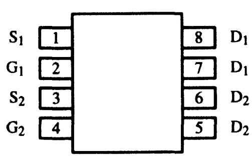
Dual N- and P-Channel 2.5-V (G-S) Rated MOSFET

Product Summary

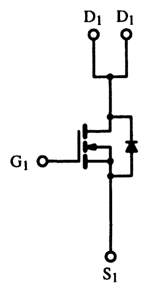
	V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
N-Channel	20	0.03 @ V_{GS} = 4.5 V	±6
		0.04 @ V_{GS} = 2.5 V	±5.2
P-Channel	–12	0.05 @ V_{GS} = –4.5 V	±5
		0.074 @ V_{GS} = –2.5 V	±4.1

2.5-V Rated

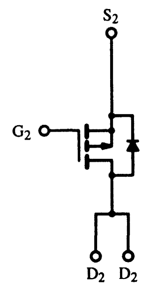
SO-8



Top View



N-Channel MOSFET



P-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage		V_{DS}	20	–12	V
Gate-Source Voltage		V_{GS}	±8	±8	V
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	±6	±5	A
	T_A = 70°C		±4.8	±4.0	A
Pulsed Drain Current		I_{DM}	±20	±20	A
Continuous Source Current (Diode Conduction)[a]		I_S	1.7	–1.7	A
Maximum Power Dissipation[a]	T_A = 25°C	P_D	2.0		W
	T_A = 70°C		1.3		W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150		°C

Thermal Resistance Ratings

Parameter	Symbol	N- or P- Channel	Unit
Maximum Junction-to-Ambient[a]	R_{thJA}	62.5	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70161.

3
SOIC-8

New Product

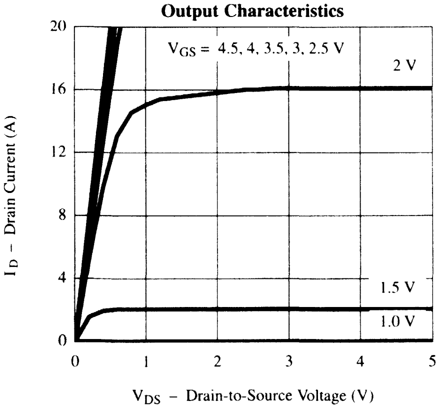
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition		Min	Typ[a]	Max	Unit
Static							
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 µA	N-Ch	0.6			V
		$V_{DS} = V_{GS}$, I_D = −250 µA	P-Ch	−0.6			
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±8 V	N-Ch			±100	nA
			P-Ch			±100	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V	N-Ch			1	µA
		V_{DS} = −12 V, V_{GS} = 0 V	P-Ch			−1	
		V_{DS} = 20 V, V_{GS} = 0 V, T_J = 55°C	N-Ch			5	
		V_{DS} = −12 V, V_{GS} = 0 V, T_J = 55°C	P-Ch			−5	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 4.5 V	N-Ch	20			A
		V_{DS} ≤ −5 V, V_{GS} = −4.5 V	P-Ch	−20			
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 4.5 V, I_D = 6 A	N-Ch		0.023	0.03	Ω
		V_{GS} = −4.5 V, I_D = −5 A	P-Ch		0.039	0.05	
		V_{GS} = 2.5 V, I_D = 5.2 A	N-Ch		0.028	0.04	
		V_{GS} = −2.5 V, I_D = −4.1 A	P-Ch		0.051	0.074	
Forward Transconductance[b]	g_{fs}	V_{DS} = 10 V, I_D = 6 A	N-Ch		24		S
		V_{DS} = −9 V, I_D = −5 A	P-Ch		16		
Diode Forward Voltage[b]	V_{SD}	I_S = 1.7 A, V_{GS} = 0 V	N-Ch		0.75	1.2	V
		I_S = −1.7 A, V_{GS} = 0 V	P-Ch		−0.75	−1.2	
Dynamic[a]							
Total Gate Charge	Q_g	N-Channel V_{DS} = 10 V, V_{GS} = 4.5 V, I_D = 6 A; P-Channel V_{DS} = −6 V, V_{GS} = −4.5 V, I_D = −5A	N-Ch		21	40	nC
			P-Ch		21	40	
Gate-Source Charge	Q_{gs}		N-Ch		2.9		
			P-Ch		3		
Gate-Drain Charge	Q_{gd}		N-Ch		6.5		
			P-Ch		6		
Turn-On Delay Time	$t_{d(on)}$	N-Channel V_{DD} = 10 V, R_L = 10 Ω, I_D ≅ 1 A, V_{GEN} = 4.5 V, R_G = 6 Ω; P-Channel V_{DD} = −10 V, R_L = 10 Ω, I_D ≅ −1 A, V_{GEN} = −4.5 V, R_G = 6 Ω	N-Ch		30	60	ns
			P-Ch		20	40	
Rise Time	t_r		N-Ch		70	140	
			P-Ch		40	80	
Turn-Off Delay Time	$t_{d(off)}$		N-Ch		70	140	
			P-Ch		100	200	
Fall Time	t_f		N-Ch		30	60	
			P-Ch		60	120	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 1.7 A, di/dt = 100 A/µs	N-Ch		70	100	
		I_F = −1.7 A, di/dt = 100 A/µs	P-Ch		67	100	

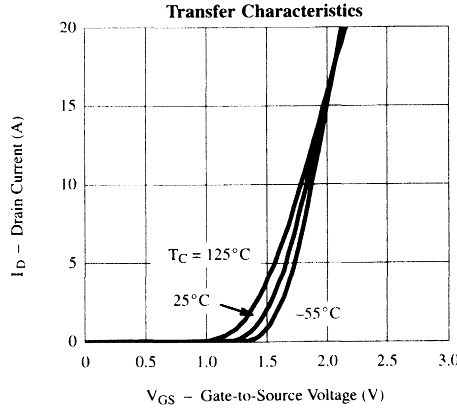
Notes
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

Typical Characteristics (25 °C Unless Otherwise Noted) N-Channel

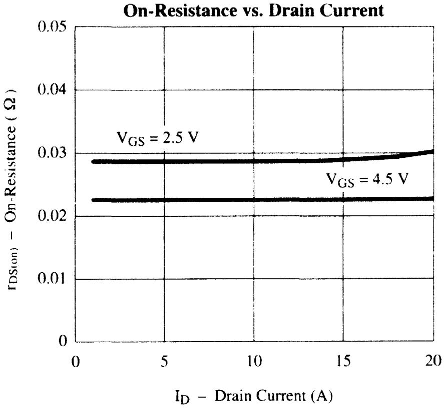
Output Characteristics



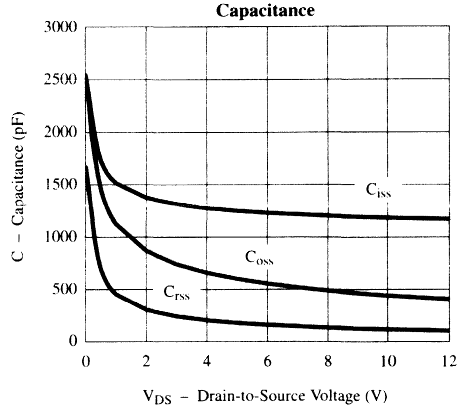
Transfer Characteristics



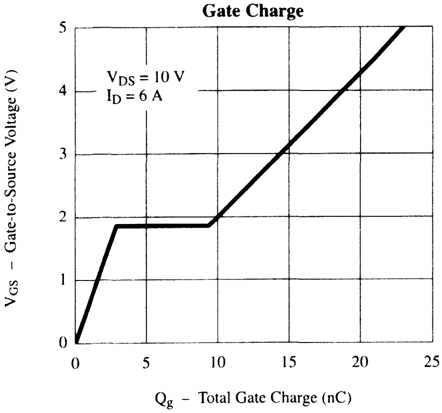
On-Resistance vs. Drain Current



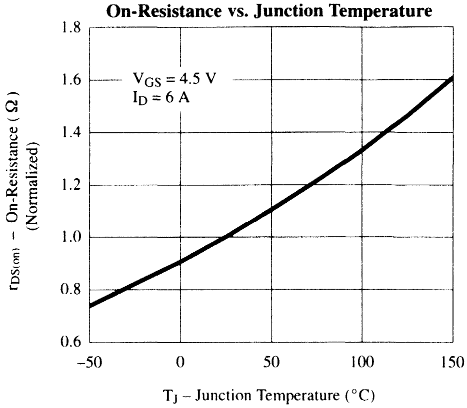
Capacitance



Gate Charge

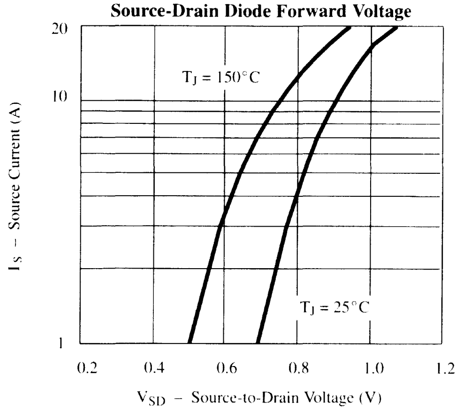


On-Resistance vs. Junction Temperature

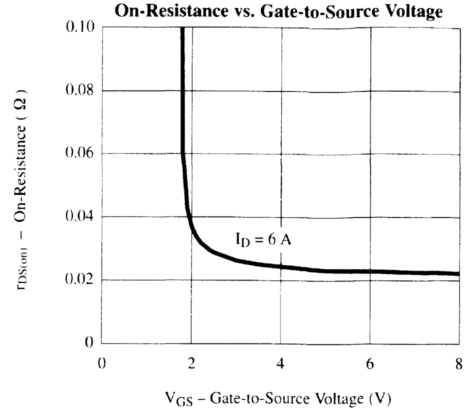


Typical Characteristics (25 °C Unless Otherwise Noted) N-Channel

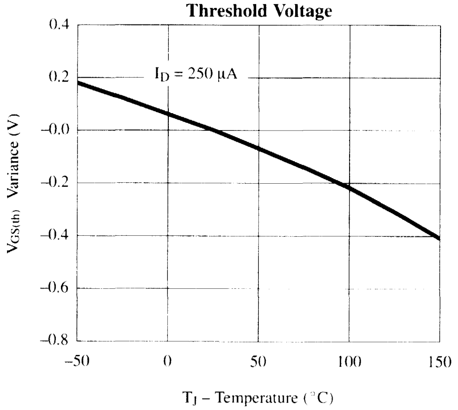
Source-Drain Diode Forward Voltage



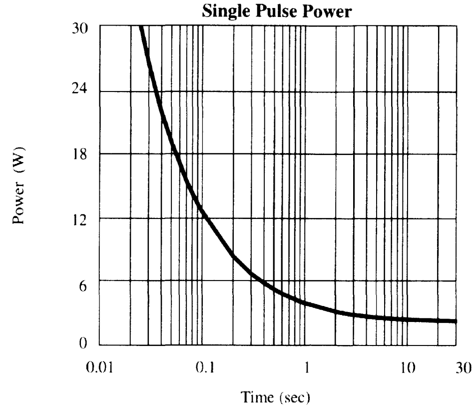
On-Resistance vs. Gate-to-Source Voltage



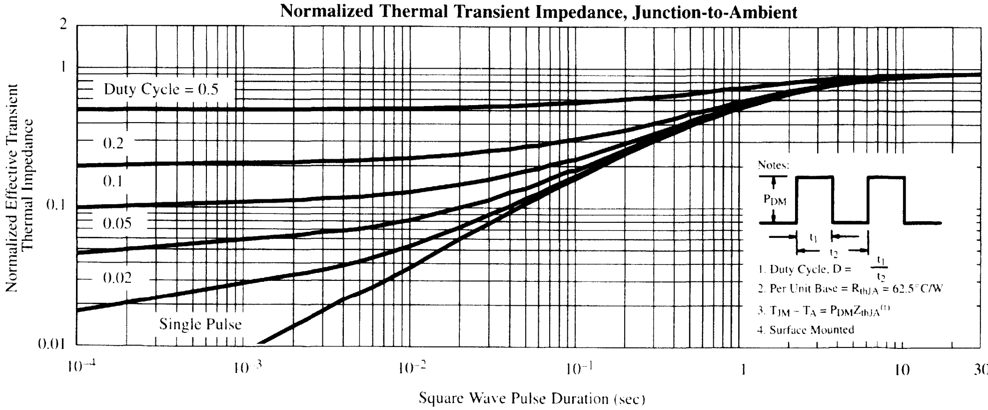
Threshold Voltage



Single Pulse Power



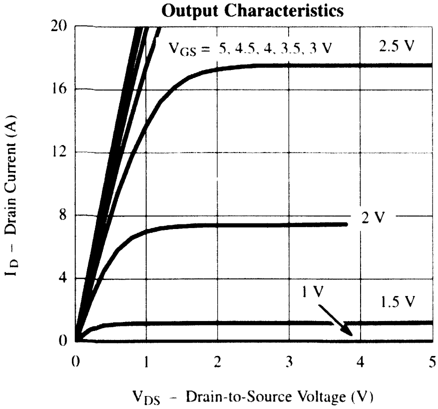
Normalized Thermal Transient Impedance, Junction-to-Ambient



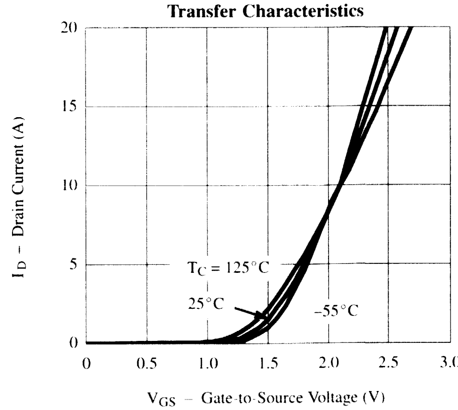
New Product

Typical Characteristics (25°C Unless Otherwise Noted) P-Channel

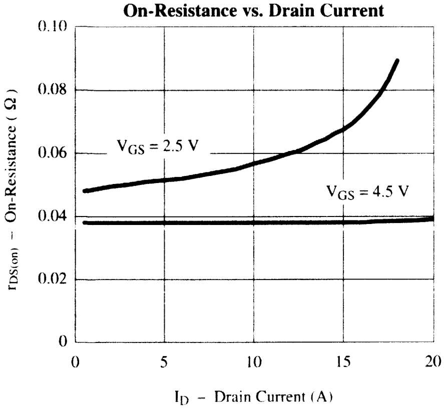
Output Characteristics



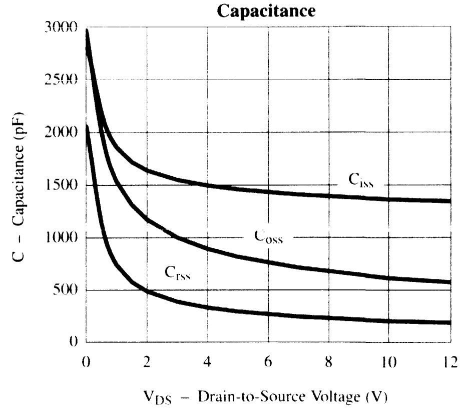
Transfer Characteristics



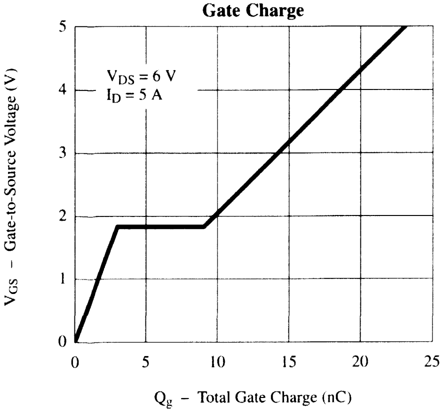
On-Resistance vs. Drain Current



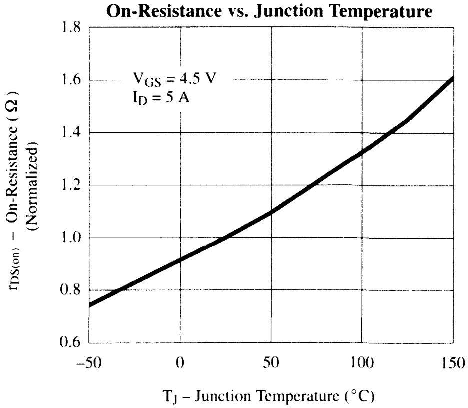
Capacitance



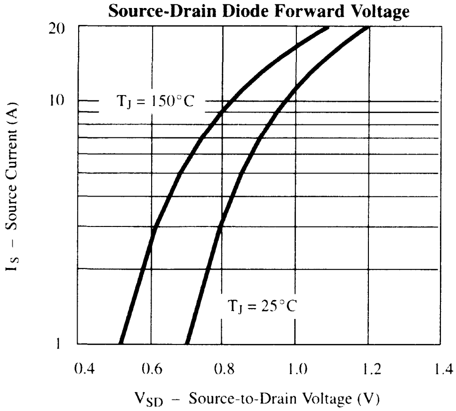
Gate Charge

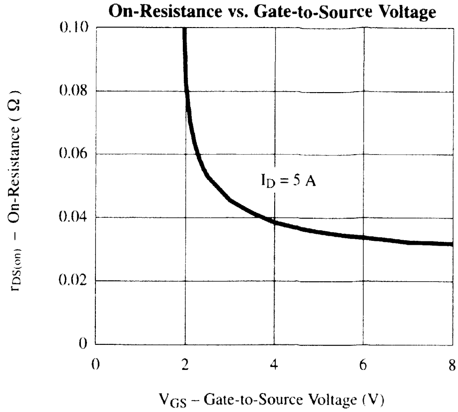


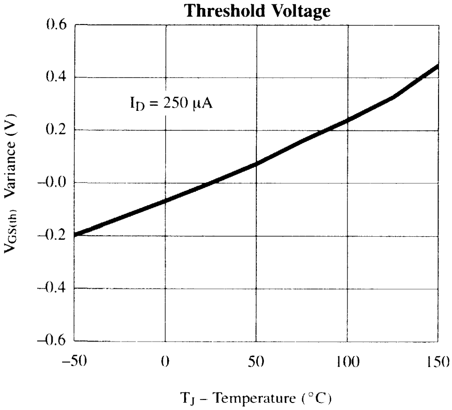
On-Resistance vs. Junction Temperature

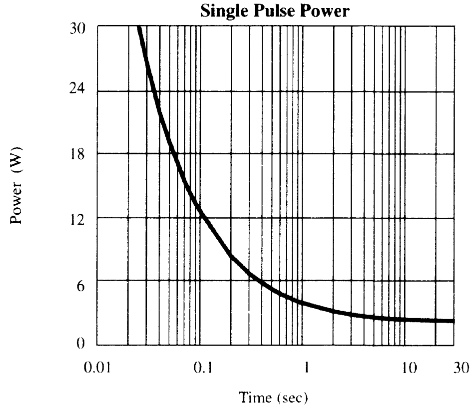


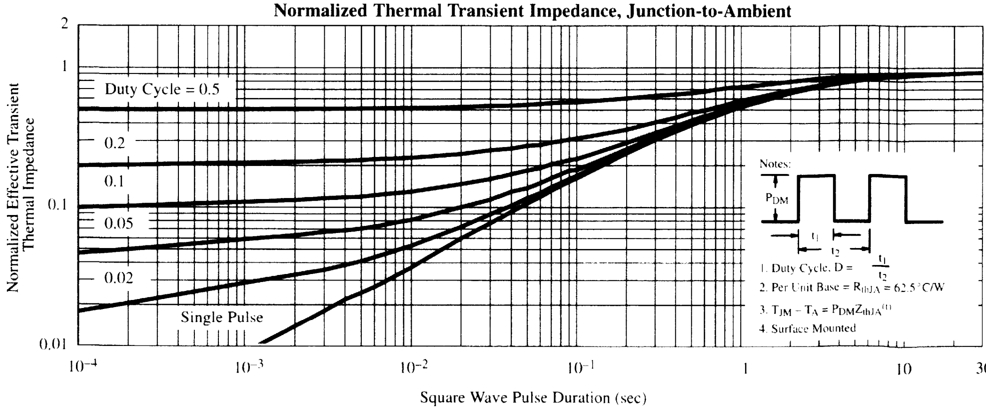
Typical Characteristics (25°C Unless Otherwise Noted) P-Channel











New Product

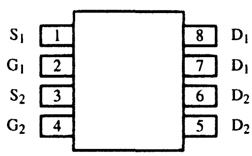
Dual N-Channel Enhancement-Mode MOSFET

Product Summary

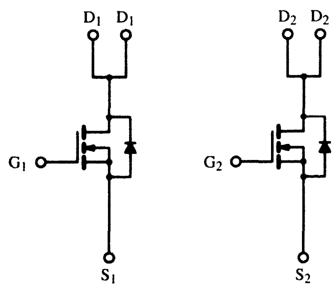
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
20	0.05 @ V_{GS} = 4.5 V	±5.0
	0.06 @ V_{GS} = 3.0 V	±4.2
	0.08 @ V_{GS} = 2.5 V	±3.6

2.5-V Rated

SO-8



Top View



N-Channel MOSFET N-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	±12	
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	±5.0	A
	T_A = 70°C		±4.0	
Pulsed Drain Current (10 µs Pulse Width)		I_{DM}	±48	
Continuous Source Current (Diode Conduction)[a]		I_S	1.7	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	2	W
	T_A = 70°C		1.3	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient[a]	R_{thJA}	62.5	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70145. A SPICE Model data sheet is available for this product (FaxBack document #70538).

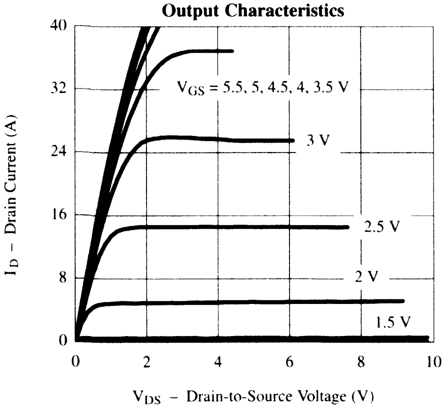
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\ \mu A$	0.8			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = \pm 12$ V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 10$ V, $V_{GS} = 0$ V			1	μA
		$V_{DS} = 16$ V, $V_{GS} = 0$ V, $T_J = 70°C$			5	
On-State Drain Current[b]	$I_{D(on)}$	$V_{DS} \geq 5$ V, $V_{GS} = 5$ V	30			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	$V_{GS} = 7.2$ V, $I_D = 5.0$ A	0.025	0.038	0.045	Ω
		$V_{GS} = 4.5$ V, $I_D = 5.0$ A		0.041	0.05	
		$V_{GS} = 3.0$ V, $I_D = 3.9$ A		0.050	0.06	
		$V_{GS} = 2.5$ V, $I_D = 1$ A		0.062	0.08	
Forward Transconductance[b]	g_{fs}	$V_{DS} = 10$ V, $I_D = 5.0$ A		14		S
Diode Forward Voltage[b]	V_{SD}	$I_S = 5.0$ A, $V_{GS} = 0$ V		0.81	1.2	V
Dynamic[a]						
Total Gate Charge	Q_g	$V_{DS} = 6$ V, $V_{GS} = 4.5$ V, $I_D = 5.0$ A		9	20	nC
Gate-Source Charge	Q_{gs}			2		
Gate-Drain Charge	Q_{gd}			2.6		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 6$ V, $R_L = 6\ \Omega$ $I_D \cong 1$ A, $V_{GEN} = 4.5$ V, $R_G = 6\ \Omega$		14	40	ns
Rise Time	t_r			13	30	
Turn-Off Delay Time	$t_{d(off)}$			35	60	
Fall Time	t_f			9	30	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 5.0$ A, di/dt = 100 A/μs		60	150	

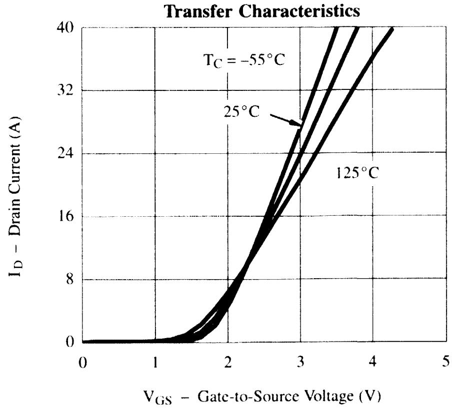
Notes
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.

Typical Characteristics (25 °C Unless Otherwise Noted)

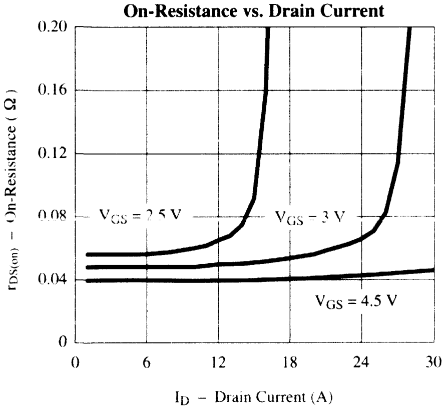
Output Characteristics



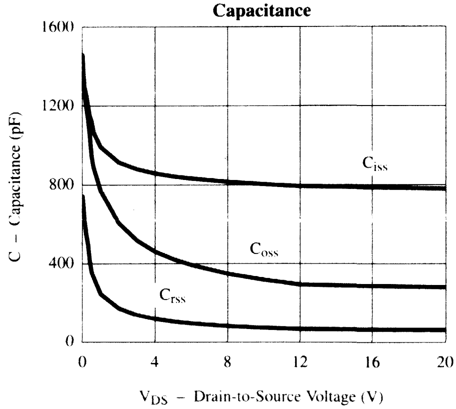
Transfer Characteristics



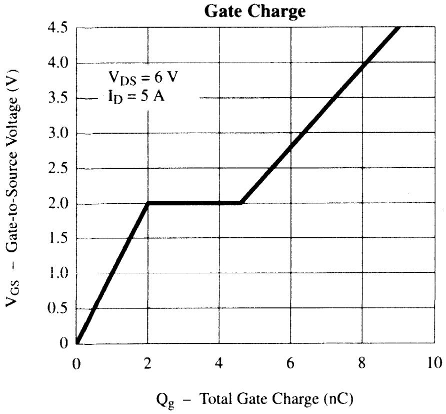
On-Resistance vs. Drain Current



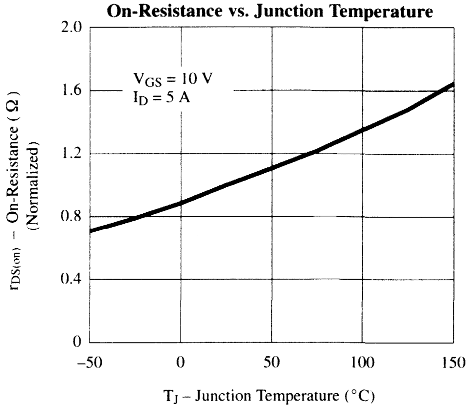
Capacitance



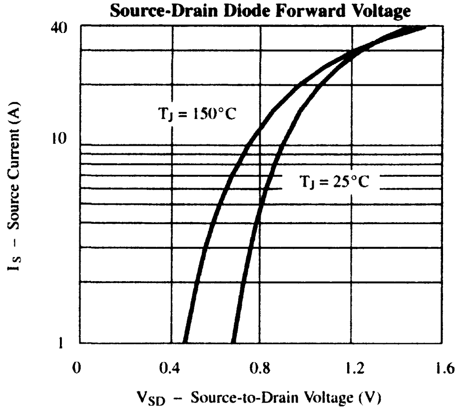
Gate Charge

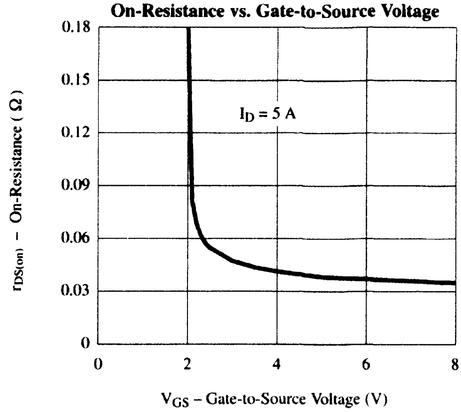


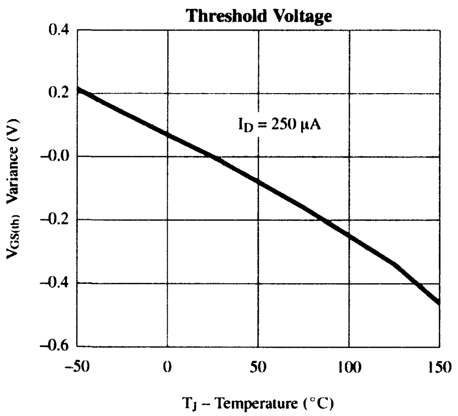
On-Resistance vs. Junction Temperature

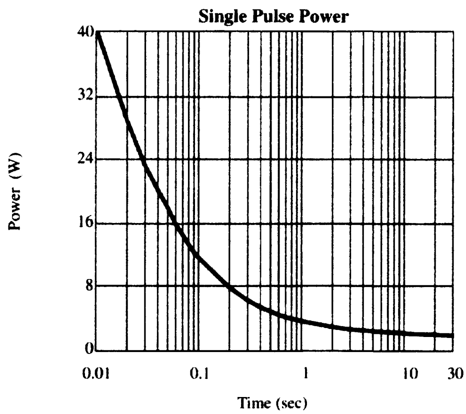


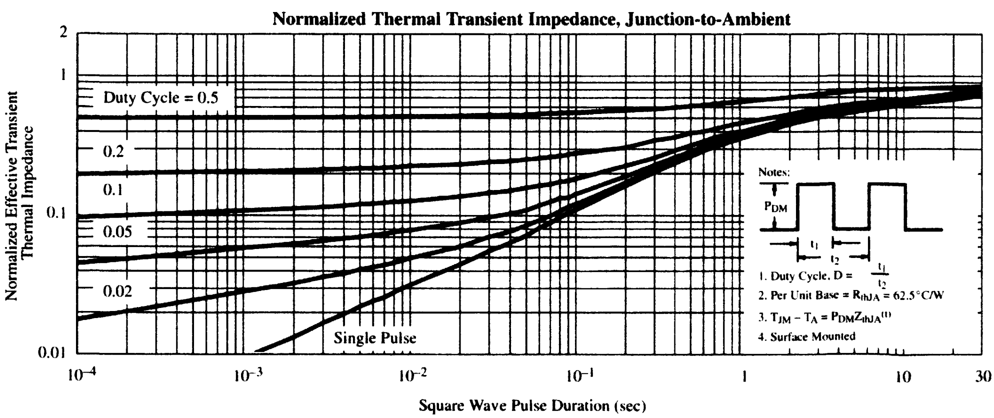
Typical Characteristics (25°C Unless Otherwise Noted)









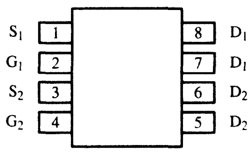


Dual N-Channel Enhancement-Mode MOSFET

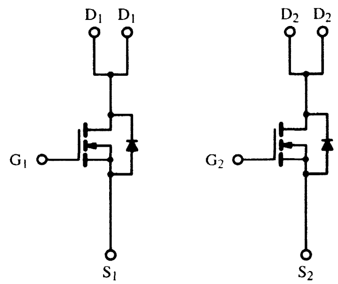
Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
20	0.03 @ V_{GS} = 4.5 V	±6
	0.04 @ V_{GS} = 2.5 V	±5.2

SO-8



Top View



N-Channel MOSFET N-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	±8	
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	±6	A
	T_A = 70°C		±4.8	
Pulsed Drain Current (10-µs Pulse Width)		I_{DM}	±20	
Continuous Source Current (Diode Conduction)[a]		I_S	1.7	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	2.0	W
	T_A = 70°C		1.3	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient[a]	R_{thJA}	62.5	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 10 sec.

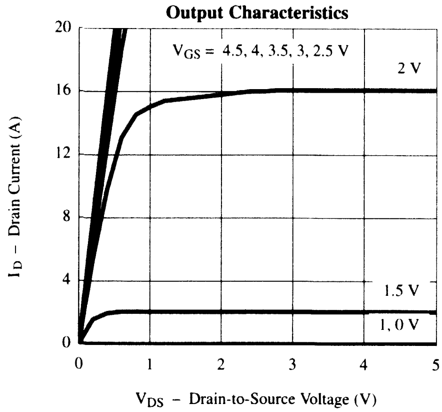
Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70162.

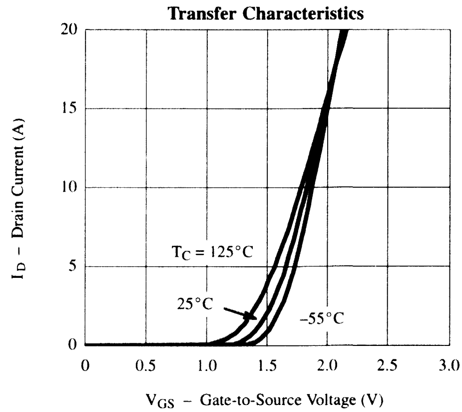
Specifications (T_J = 25°C Unless Otherwise Noted)

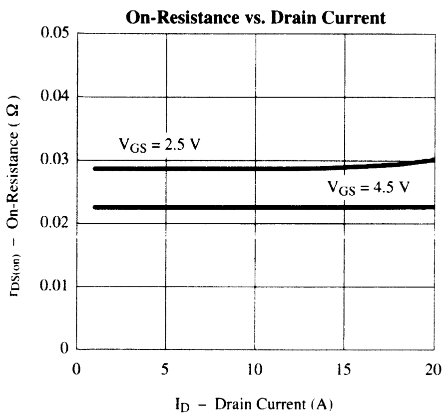
Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static–0.6						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 µA	0.6			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 8 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V			–1	µA
		V_{DS} = 20 V, V_{GS} = 0 V, T_J = 55°C			–5	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 4.5 V	20			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 4.5 V, I_D = 6 A		0.023	0.03	Ω
		V_{GS} = 2.5 V, I_D = 5.2 A		0.028	0.04	
Forward Transconductance[b]	g_{fs}	V_{DS} = 10 V, I_D = 6 A		24		S
Diode Forward Voltage[b]	V_{SD}	I_S = 1.7 A, V_{GS} = 0 V		0.75	1.2	V
Dynamic[a]						
Total Gate Charge	Q_g	V_{DS} = 10 V, V_{GS} = 4.5 V, I_D = 6 A		21	40	nC
Gate-Source Charge	Q_{gs}			2.9		
Gate-Drain Charge	Q_{gd}			6.5		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 10 V, R_L = 10 Ω I_D ≅ 1 A, V_{GEN} = 4.5 V, R_G = 6 Ω		30	60	ns
Rise Time	t_r			70	140	
Turn-Off Delay Time	$t_{d(off)}$			70	140	
Fall Time	t_f			30	60	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 1.7 A, di/dt = 100 A/µs		70	100	

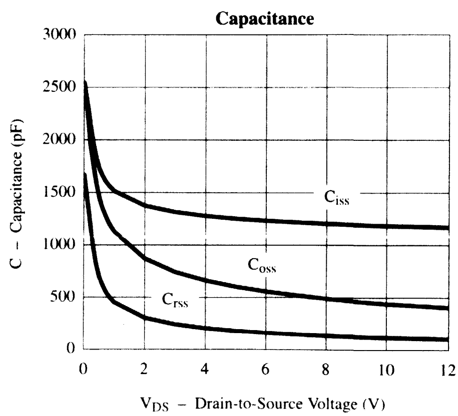
Notes
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

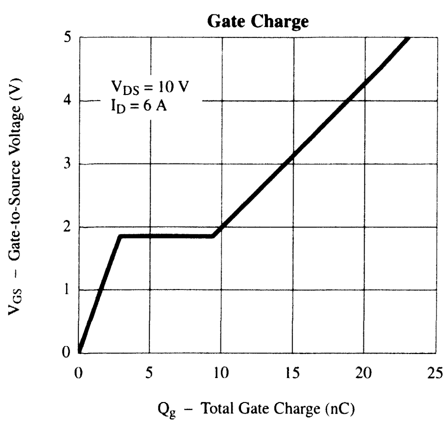
Typical Characteristics (25 °C Unless Otherwise Noted)

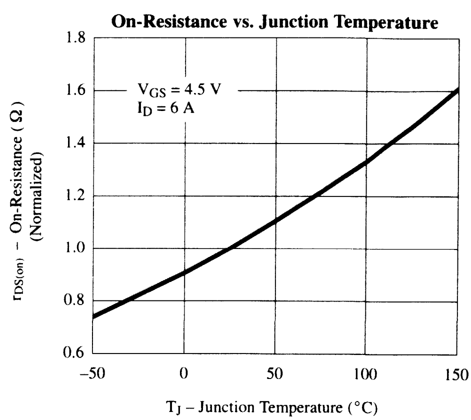






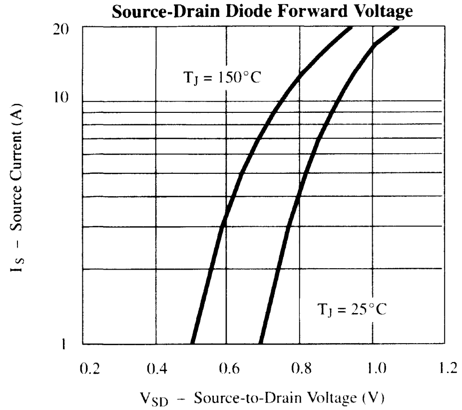




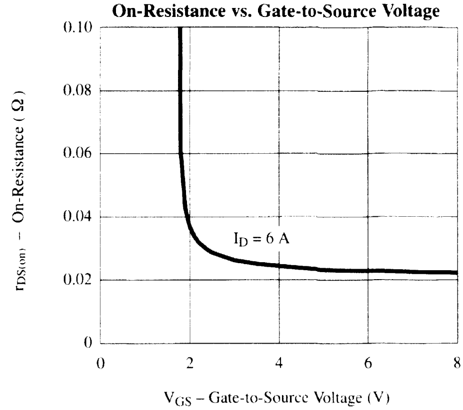


Typical Characteristics (25°C Unless Otherwise Noted)

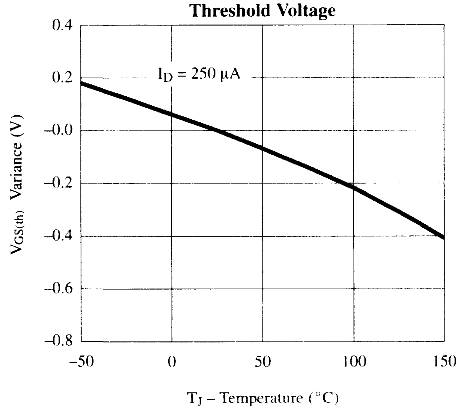
Source-Drain Diode Forward Voltage



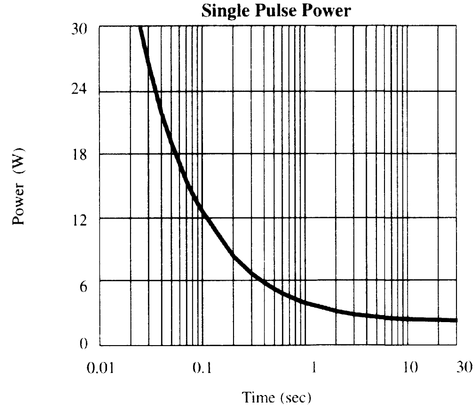
On-Resistance vs. Gate-to-Source Voltage



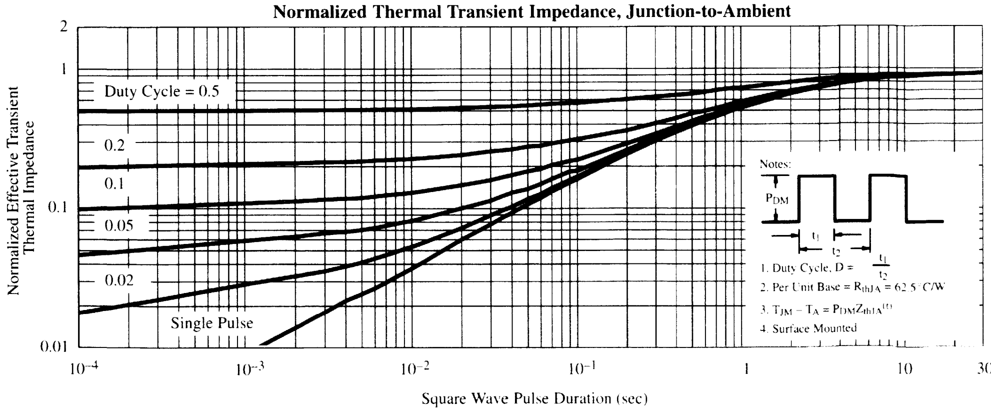
Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient



New Product

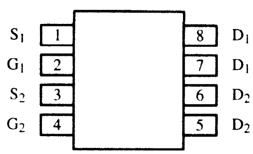
Dual P-Channel 2.5-V (G-S) Rated MOSFET

Product Summary

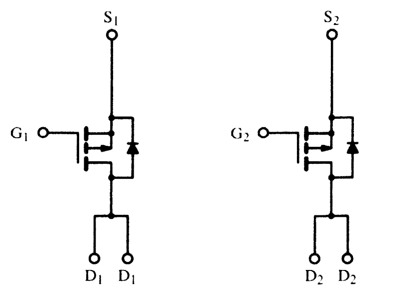
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
–12	0.05 @ V_{GS} = –4.5 V	± 5
	0.074 @ V_{GS} = –2.5 V	± 4.1

2.5-V Rated

SO-8



Top View



P-Channel MOSFET P-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	–12	V
Gate-Source Voltage		V_{GS}	± 8	
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	± 5	A
	T_A = 70°C		± 4.0	
Pulsed Drain Current (10-µs Pulse Width)		I_{DM}	± 20	
Continuous Source Current (Diode Conduction)[a]		I_S	–1.7	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	2.0	W
	T_A = 70°C		1.3	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient[a]	R_{thJA}	62.5	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70163.
A SPICE Model data sheet is available for this product (FaxBack document #70569).

New Product

Specifications (T_J = 25 °C Unless Otherwise Noted)

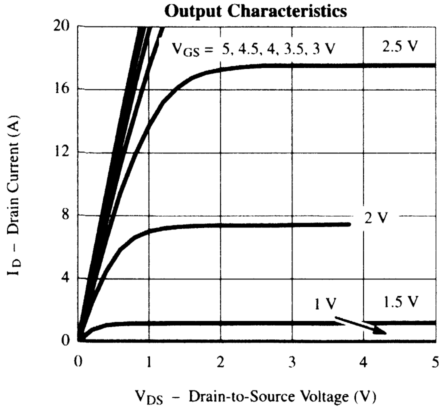
Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static–0.6						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = –250 µA	–0.6			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 8 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = –12 V, V_{GS} = 0 V			–1	µA
		V_{DS} = –12 V, V_{GS} = 0 V, T_J = 55°C			–5	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = –4.5 V	–20			A
		V_{DS} ≥ 5 V, V_{GS} = –2.5 V	–6			
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = –4.5 V, I_D = –5 A		0.039	0.05	Ω
		V_{GS} = –2.5 V, I_D = –3 A		0.051	0.074	
Forward Transconductance[b]	g_{fs}	V_{DS} = –9 V, I_D = –5 A		16		S
Diode Forward Voltage[b]	V_{SD}	I_S = –1.7 A, V_{GS} = 0 V		–0.75	–1.2	V
Dynamic[a]						
Total Gate Charge	Q_g	V_{DS} = –6 V, V_{GS} = –4.5 V, I_D = –5 A		21	40	nC
Gate-Source Charge	Q_{gs}			3		
Gate-Drain Charge	Q_{gd}			6		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = –6 V, R_L = 6 Ω I_D ≅ –1 A, V_{GEN} = –4.5 V, R_G = 6 Ω		20	40	ns
Rise Time	t_r			40	80	
Turn-Off Delay Time	$t_{d(off)}$			100	200	
Fall Time	t_f			60	120	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = –1.7 A, di/dt = 100 A/µs		67	100	

Notes
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

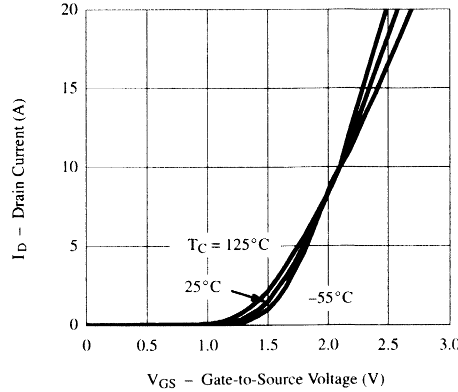
New Product

Typical Characteristics (25°C Unless Otherwise Noted)

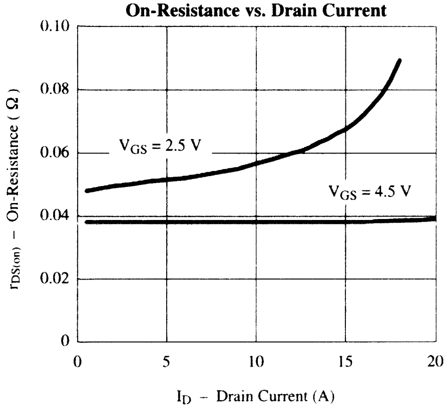
Output Characteristics



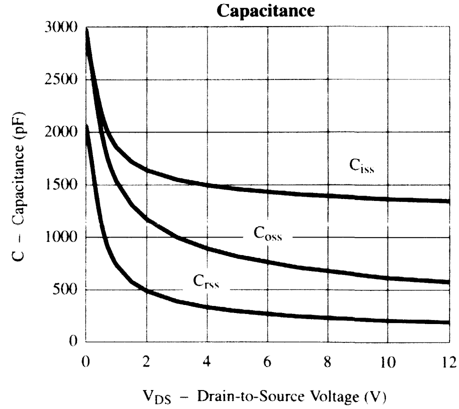
Transfer Characteristics



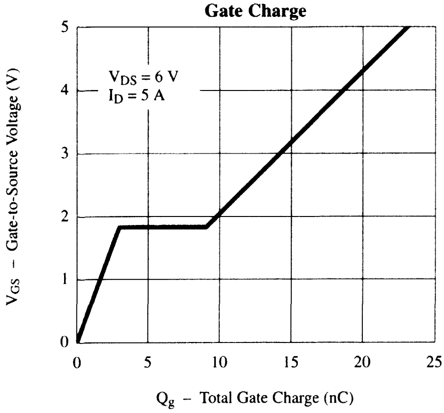
On-Resistance vs. Drain Current



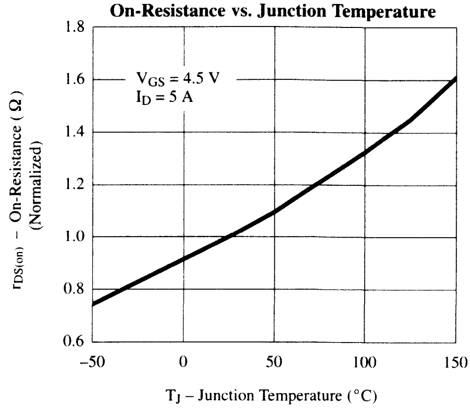
Capacitance



Gate Charge



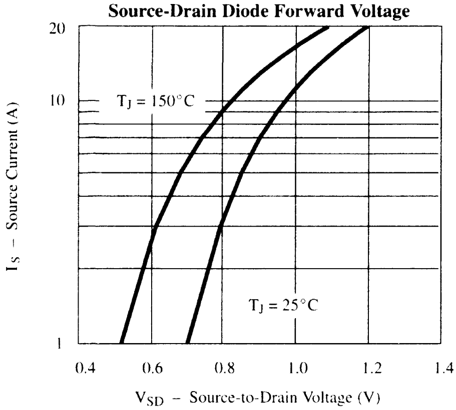
On-Resistance vs. Junction Temperature



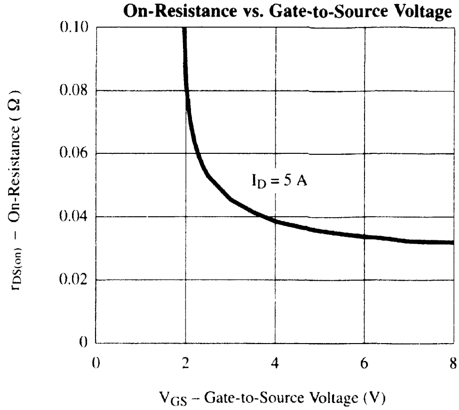
New Product

Typical Characteristics (25°C Unless Otherwise Noted)

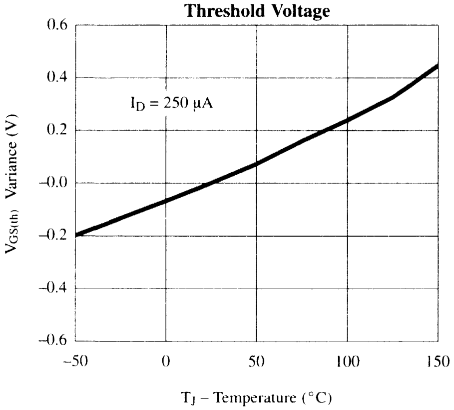
Source-Drain Diode Forward Voltage



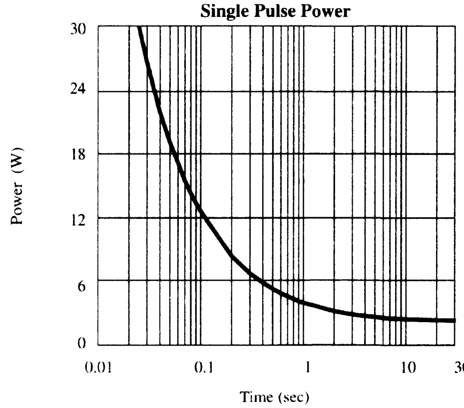
On-Resistance vs. Gate-to-Source Voltage



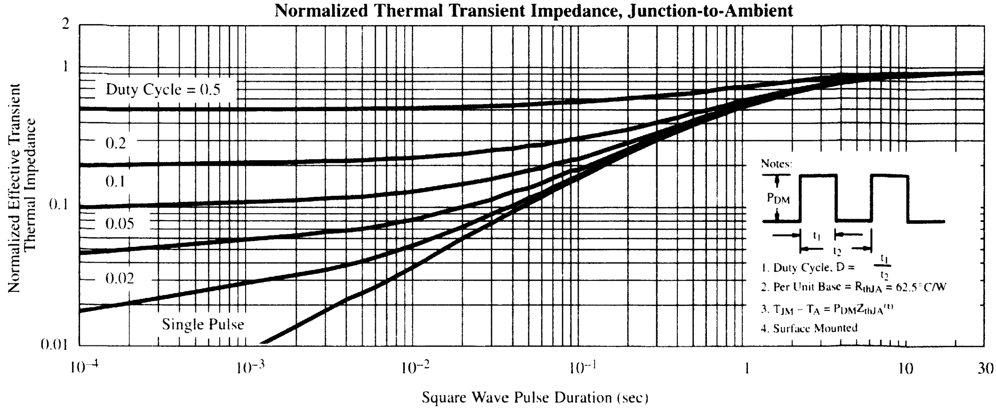
Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient



Power MOSFETs Optimized for Low-Voltage DC/DC Conversion

Designers of low-voltage dc-to-dc converters have two main concerns: reducing size and reducing losses. As a way of reducing size, designers are increasing switching frequencies. But the result has often been reduced converter efficiency. To minimize losses, MOSFET manufacturers have generally focused on lowering on-resistance. But the results have not been optimal for dc-to-dc conversion designs, since gate charge and switching speed issues have been largely ignored. The dominant losses associated with MOSFETs were once conduction losses, but this is no longer the case.

TEMIC's new family of PWM optimized MOSFETs are designed to give the highest efficiency available for a given on-resistance in switching applications such as dc-to-dc conversion. These new devices provide a very low gate charge per unit of on-resistance, in addition to fast switching times. The result is reduced gate drive and crossover losses, allowing designers of dc-to-dc converters to simultaneously to reduce design size and increase efficiency.

Figure of Merit for PWM Optimized MOSFET Technology

Normalized gate charge serves as a quick figure of merit for comparing the PWM optimized, conventional, and low-threshold MOSFETs technologies. This was calculated by normalizing the on-resistance and gate charge of the n-channel MOSFET to 100 mΩ:

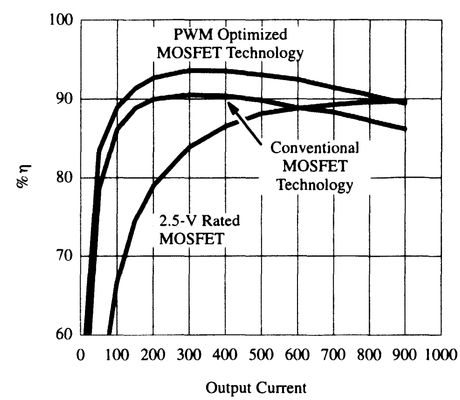
Type of MOSFET	Typical On-Resistance at 4.5 V (mΩ)	Specific Gate Charge	Normalized Gate Charge per 100 mΩ (nC)
PWM Optimized	120	1.7	1.4
Conventional	100	4.0	4.0
2.5-V Rated	73	16.0	22.0

Similar performance advantages will be seen for the p-channel process as well.

Ideal applications for TEMIC's PWM optimized MOSFETs include mobile communication equipment and other hand-held battery-operated systems. An example of the efficiency gains achieved with this technology is shown below.

Efficiency comparison between high-frequency, conventional, and low-threshold MOSFETs at a switching frequency of 1 MHz.

If you would like to review a detailed application note, call our FaxBack system at 408-970-5600 and refer to document number 70649.



4

High-Efficiency

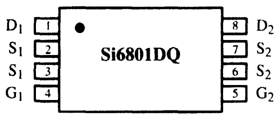
Dual N- and P-Channel, Reduced Q_g, Fast Switching MOSFET

Product Summary

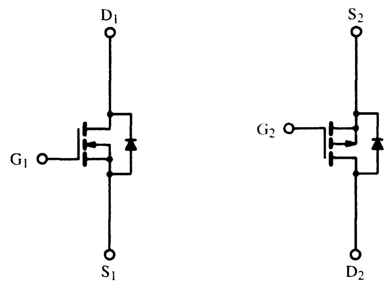
	V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
N-Channel	20	0.160 @ V_{GS} = 4.5 V	± 1.9
		0.260 @ V_{GS} = 3.0 V	± 1.5
P-Channel	–20	0.190 @ V_{GS} = –4.5 V	± 1.7
		0.280 @ V_{GS} = –3.0 V	± 1.3

High-Efficiency
PWM Optimized

TSSOP-8



Top View



N-Channel MOSFET P-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage		V_{DS}	20	–20	V
Gate-Source Voltage		V_{GS}	± 12		V
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	± 1.9	± 1.7	A
	T_A = 70°C		± 1.5	± 1.3	A
Pulsed Drain Current		I_{DM}	± 8		A
Continuous Source Current (Diode Conduction)[a]		I_S	1.0	–1.0	A
Maximum Power Dissipation[a]	T_A = 25°C	P_D	1.0		W
	T_A = 70°C		0.64		W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150		°C

Thermal Resistance Ratings

Parameter	Symbol	N- or P-Channel	Unit
Maximum Junction-to-Ambient[a]	R_{thJA}	125	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70187.

New Product

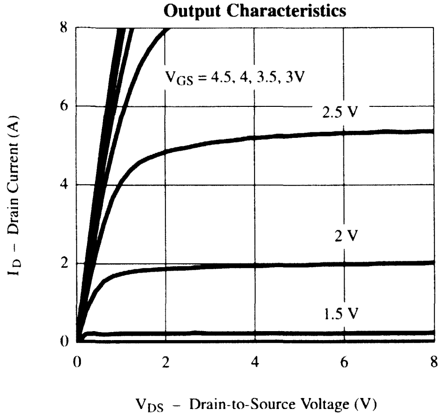
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Static							
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\ \mu A$	N-Ch	0.6			V
		$V_{DS} = V_{GS}$, $I_D = -250\ \mu A$	P-Ch	–0.6			
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = \pm 12$ V	N-Ch			± 100	nA
			P-Ch			± 100	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20$ V, $V_{GS} = 0$ V	N-Ch			1	µA
		$V_{DS} = -20$ V, $V_{GS} = 0$ V	P-Ch			–1	
		$V_{DS} = 20$ V, $V_{GS} = 0$ V, $T_J = 70°C$	N-Ch			25	
		$V_{DS} = -20$ V, $V_{GS} = 0$ V, $T_J = 70°C$	P-Ch			–25	
On-State Drain Current[b]	$I_{D(on)}$	$V_{DS} = 5$ V, $V_{GS} = 4.5$ V	N-Ch	6			A
		$V_{DS} = -5$ V, $V_{GS} = -4.5$ V	P-Ch	–6			
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	$V_{GS} = 4.5$ V, $I_D = 1.9$ A	N-Ch		0.120	0.160	Ω
		$V_{GS} = -4.5$ V, $I_D = 1.7$ A	P-Ch		0.155	0.190	
		$V_{GS} = 3.0$ V, $I_D = 1.5$ A	N-Ch		0.160	0.260	
		$V_{GS} = -3.0$ V, $I_D = 1.3$ A	P-Ch		0.210	0.280	
Forward Transconductance[b]	g_{fs}	$V_{DS} = 15$ V, $I_D = 1.9$ A	N-Ch		5.4		S
		$V_{DS} = -15$ V, $I_D = -1.7$ A	P-Ch		4.0		
Diode Forward Voltage[b]	V_{SD}	$I_S = 1.0$ A, $V_{GS} = 0$ V	N-Ch		0.77	1.2	V
		$I_S = -1.0$ A, $V_{GS} = 0$ V	P-Ch		–0.77	–1.2	
Dynamic[a]							
Total Gate Charge	Q_g	N-Channel $V_{DS} = 3.5$ V, $V_{GS} = 4.5$ V, $I_D = 0.3$ A P-Channel $V_{DS} = -3.5$ V, $V_{GS} = -4.5$ V $I_D = -0.3$ A	N-Ch		1.7	3.5	nC
			P-Ch		3.5	7.0	
Gate-Source Charge	Q_{gs}		N-Ch		0.26		
			P-Ch		0.76		
Gate-Drain Charge	Q_{gd}		N-Ch		0.41		
			P-Ch		0.70		
Turn-On Delay Time	$t_{d(on)}$	N-Channel $V_{DD} = 3.5$ V, $R_L = 11.5\ \Omega$ $I_D \cong 0.3$ A, $V_{GEN} = 4.5$ V, $R_G = 6\ \Omega$ P-Channel $V_{DD} = -3.5$ V, $R_L = 11.5\ \Omega$ $I_D \cong -0.3$ A, $V_{GEN} = -4.5$ V, $R_G = 6\ \Omega$	N-Ch		7.3	15	ns
			P-Ch		6.0	15	
Rise Time	t_r		N-Ch		10.0	20.0	
			P-Ch		10.0	20.0	
Turn-Off Delay Time	$t_{d(off)}$		N-Ch		11.0	20.0	
			P-Ch		10.0	20.0	
Fall Time	t_f		N-Ch		6.0	15	
			P-Ch		7.0	15	
Source-Drain Reverse Recovery Time	t_{rr}	N-Channel—$I_F = 1.0$ A, di/dt = 100 A/µs	N-Ch		31	60	
		P-Channel—$I_F = -1.0$ A, di/dt = 100 A/µs	P-Ch		35	60	

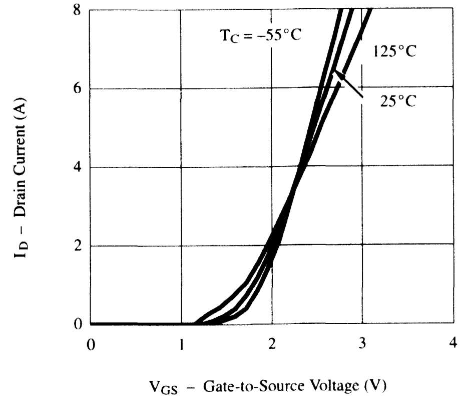
Notes
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

Typical Characteristics (25°C Unless Noted) — N-Channel

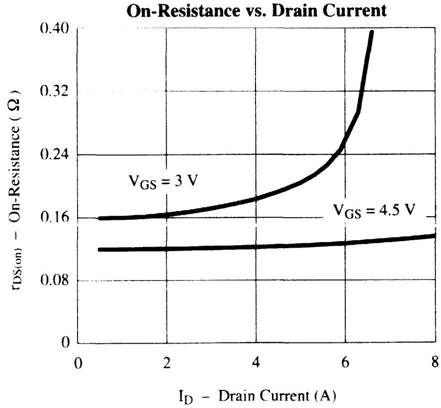
Output Characteristics



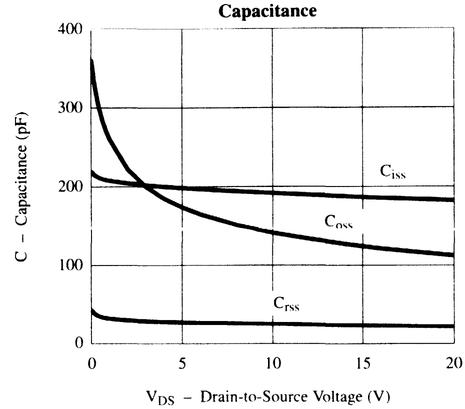
Transfer Characteristics



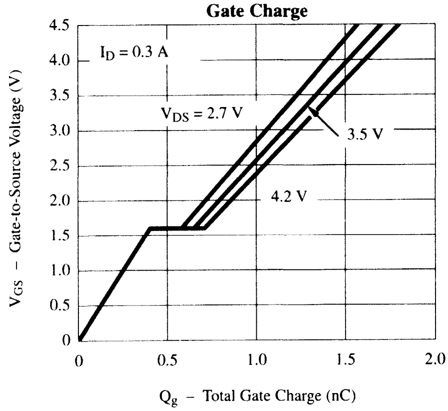
On-Resistance vs. Drain Current



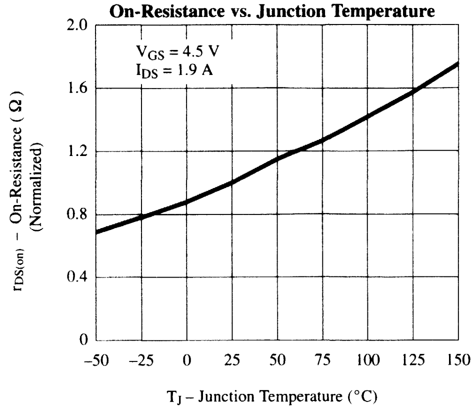
Capacitance



Gate Charge



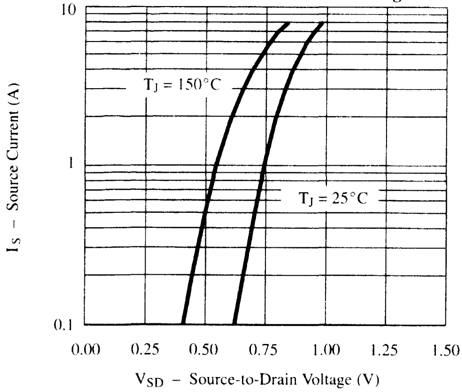
On-Resistance vs. Junction Temperature

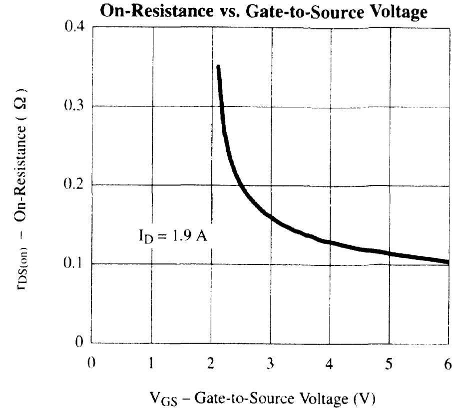


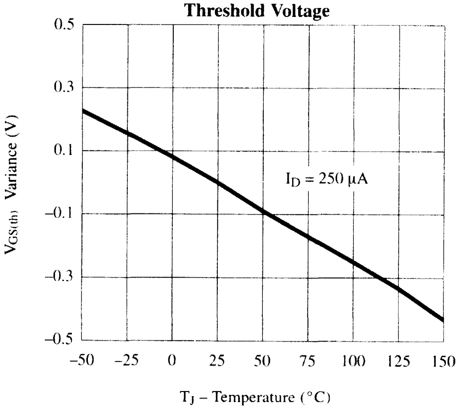
New Product

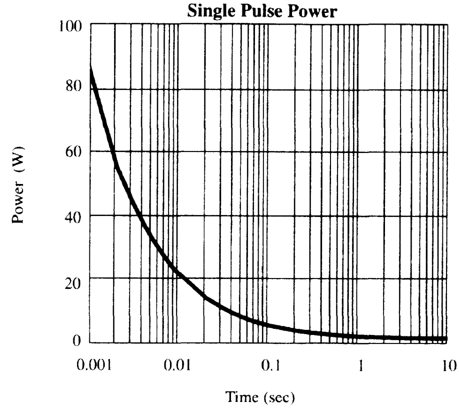
Typical Characteristics (25°C Unless Noted)

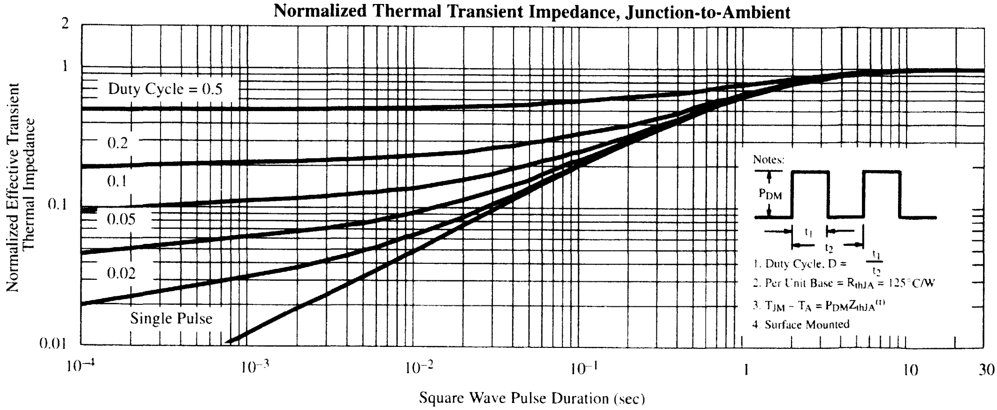
N-Channel





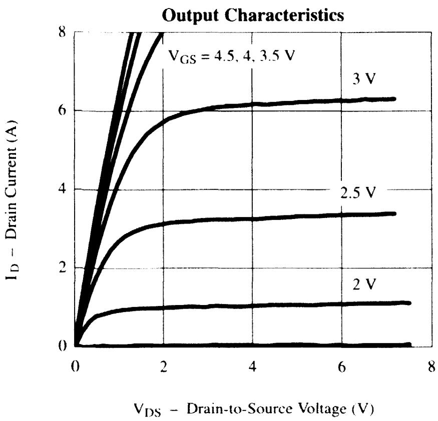


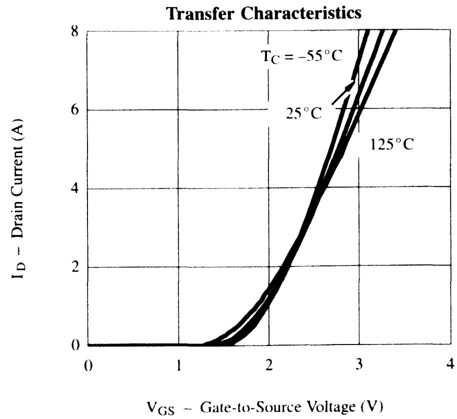


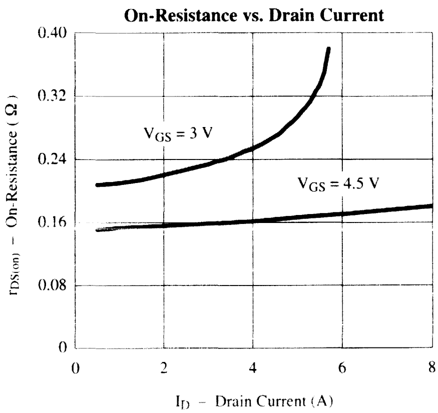


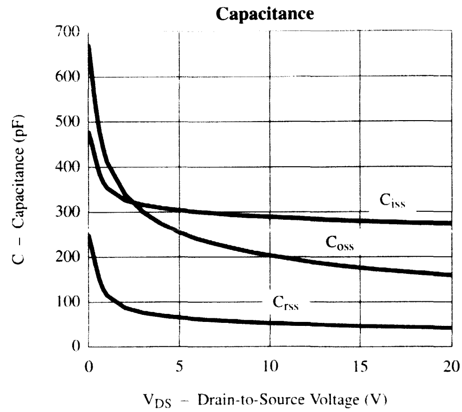
New Product

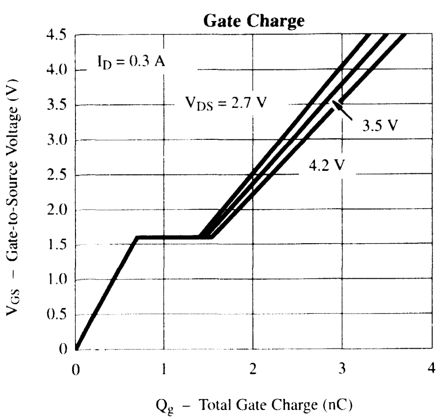
Typical Characteristics (25°C Unless Noted) P-Channel

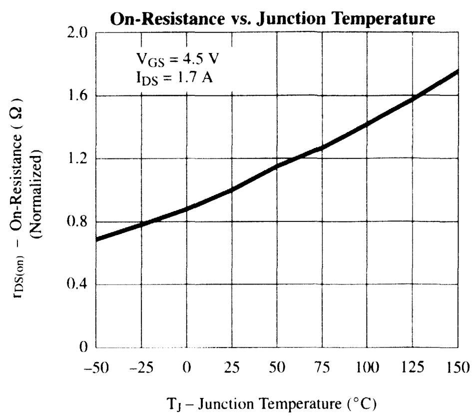








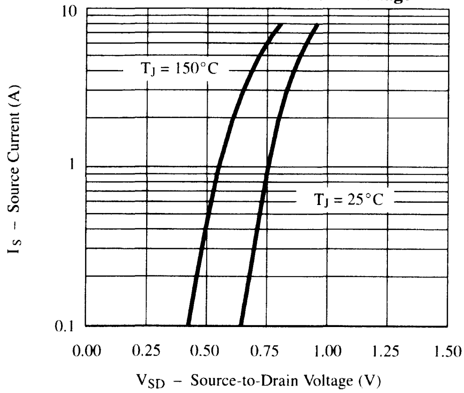




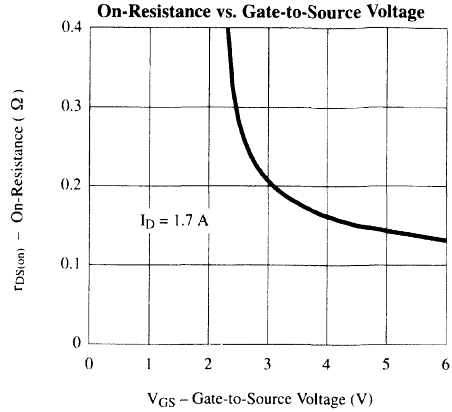
Typical Characteristics (25°C Unless Noted)

P-Channel

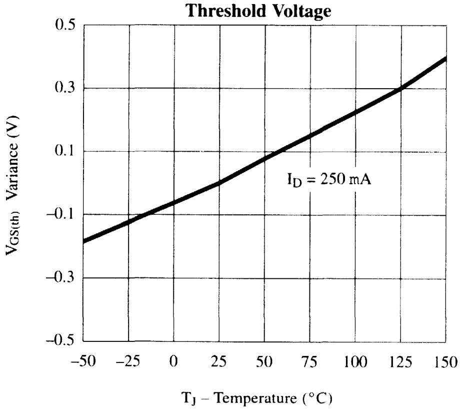
Source-Drain Diode Forward Voltage



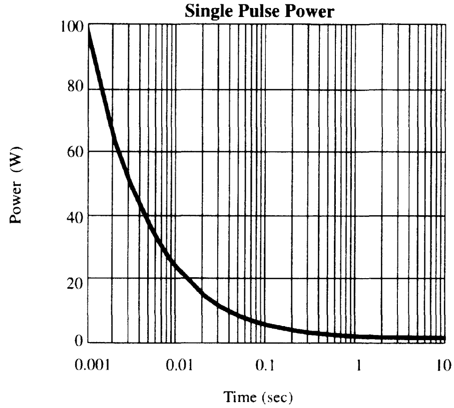
On-Resistance vs. Gate-to-Source Voltage



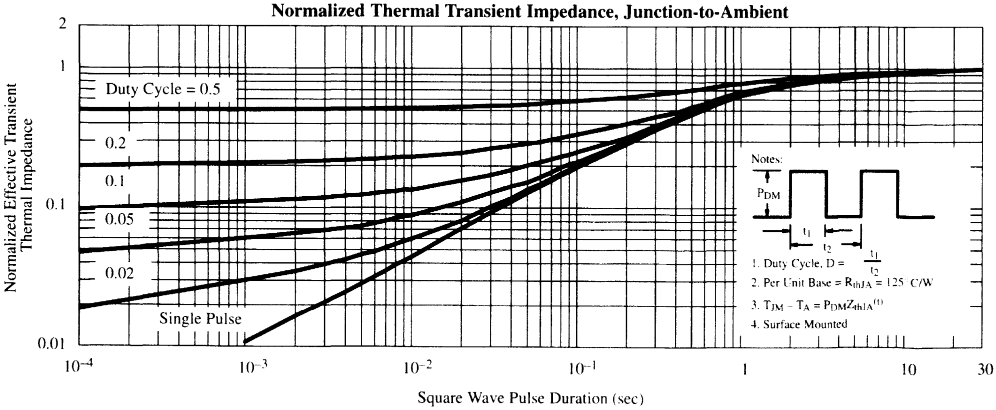
Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient



New Product

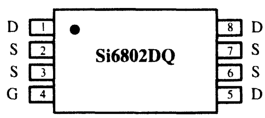
N-Channel, Reduced Q_g, Fast Switching MOSFET

Product Summary

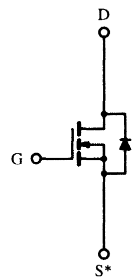
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
20	0.075 @ V_{GS} = 4.5 V	±3.3
	0.110 @ V_{GS} = 3.0 V	±2.7

High-Efficiency
PWM Optimized

TSSOP-8



Top View



*Source Pins 2, 3, 6, and 7 must be tied common.

N-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	±12	
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	±3.3	A
	T_A = 70°C		±2.6	
Pulsed Drain Current		I_{DM}	±20	
Continuous Source Current (Diode Conduction)[a]		I_S	1.25	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	1.5	W
	T_A = 70°C		1.0	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient[a]	R_{thJA}	83	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70188.

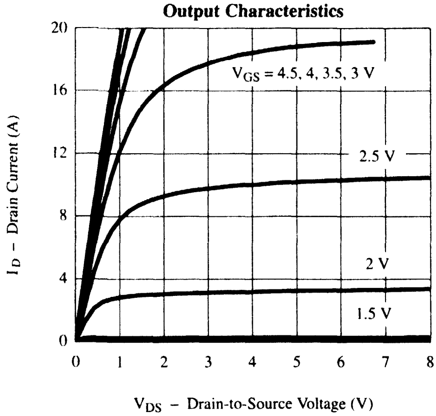
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 µA	0.6			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 12 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V			1	µA
		V_{DS} = 20 V, V_{GS} = 0 V, T_J = 70°C			25	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 4.5 V	15			A
		V_{DS} ≥ 5 V, V_{GS} = 3.0 V	6			
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 4.5 V, I_D = 3.3 A		0.048	0.075	Ω
		V_{GS} = 3.0 V, I_D = 2.7 A		0.067	0.110	
Forward Transconductance[b]	g_{fs}	V_{DS} = 10 V, I_D = 3.3 A		10.3		S
Diode Forward Voltage[b]	V_{SD}	I_S = 1.25 A, V_{GS} = 0 V		0.7	1.2	V
Dynamic[a]						
Total Gate Charge	Q_g	V_{DS} = 6 V, V_{GS} = 4.5 V, I_D = 0.3 A		4.5	9.0	nC
Gate-Source Charge	Q_{gs}			1.0		
Gate-Drain Charge	Q_{gd}			0.7		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 6 V, R_L = 20 Ω I_D ≅ 0.3 A, V_{GEN} = 4.5 V, R_G = 6 Ω		8	20	ns
Rise Time	t_r			6	15	
Turn-Off Delay Time	$t_{d(off)}$			12	25	
Fall Time	t_f			16	30	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 1.25 A, di/dt = 100 A/µs		52	80	

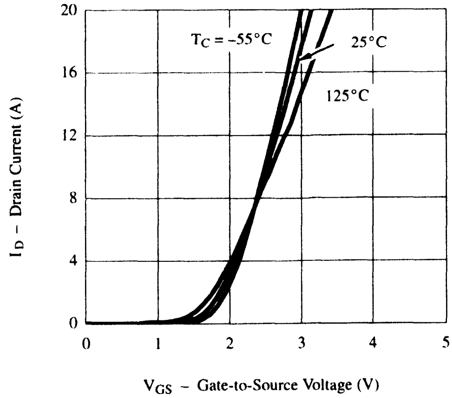
Notes
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

Typical Characteristics (25 °C Unless Otherwise Noted)

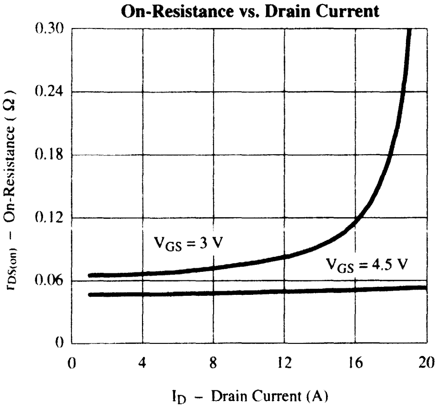
Output Characteristics



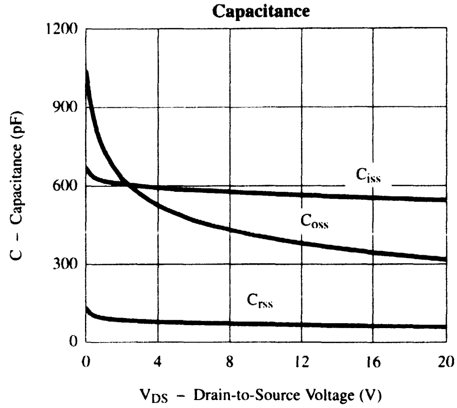
Transfer Characteristics



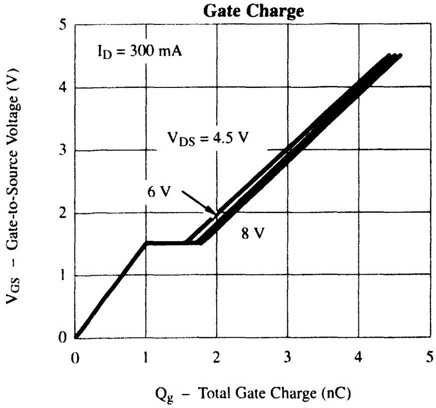
On-Resistance vs. Drain Current



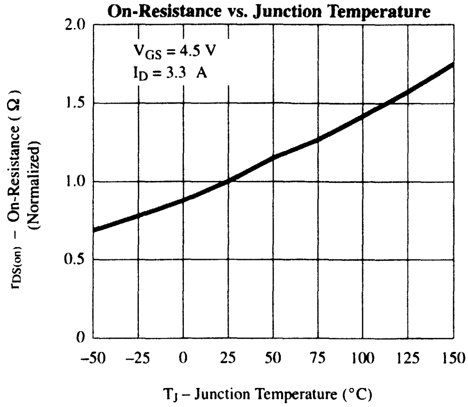
Capacitance



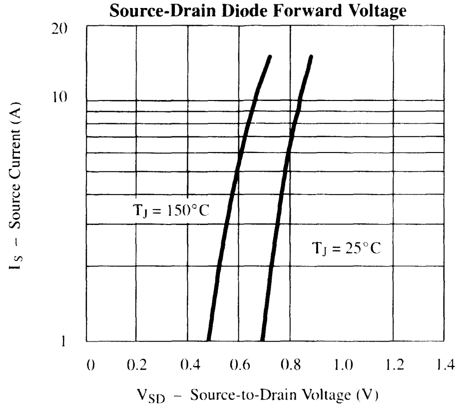
Gate Charge

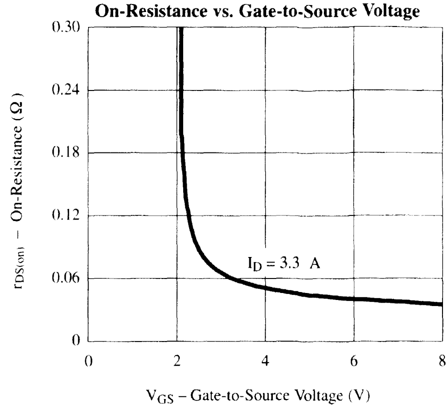


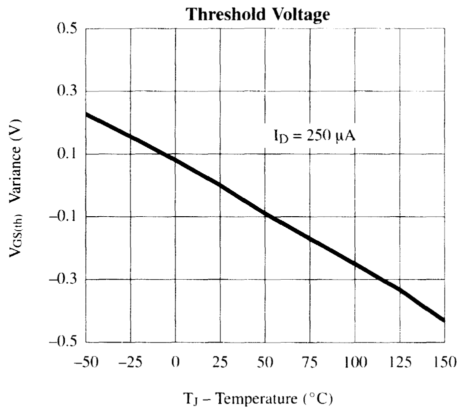
On-Resistance vs. Junction Temperature

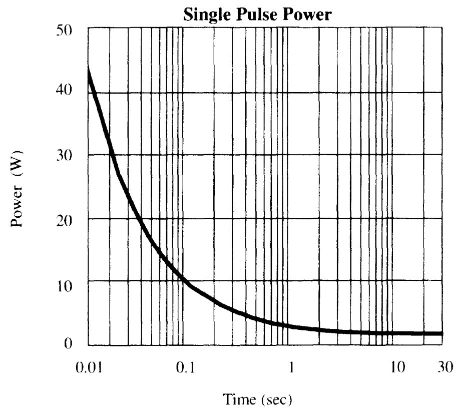


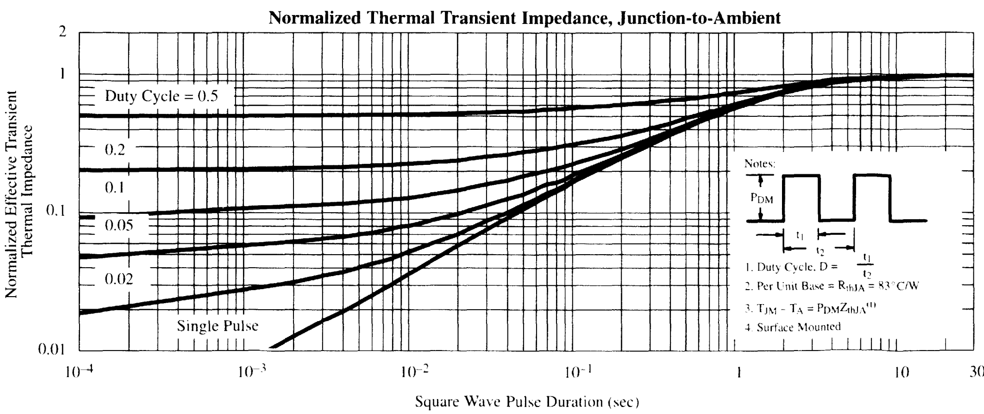
Typical Characteristics (25 °C Unless Otherwise Noted)











New Product

Si9801DY

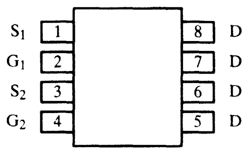
N- and P-Channel, Reduced Q_g, Fast Switching Half-Bridge

Product Summary

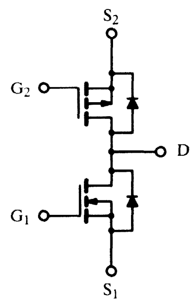
	V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
N-Channel	20	0.055 @ V_{GS} = 4.5 V	± 4.5
		0.075 @ V_{GS} = 3.0 V	± 3.8
P-Channel	–20	0.080 @ V_{GS} = –4.5 V	± 4.0
		0.120 @ V_{GS} = –3.0 V	± 3.0

High-Efficiency
PWM Optimized

SO-8



Top View



Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage		V_{DS}	20	–20	V
Gate-Source Voltage		V_{GS}	± 12		
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	± 4.5	± 4.0	A
	T_A = 70°C		± 3.6	± 3.0	
Pulsed Drain Current		I_{DM}	± 20		
Continuous Source Current (Diode Conduction)[a]		I_S	1.7	–1.7	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	2.0		W
	T_A = 70°C		1.3		
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150		°C

Thermal Resistance Ratings

Parameter	Symbol	N- or P-Channel	Unit
Maximum Junction-to-Ambient[a]	R_{thJA}	62.5	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70630.

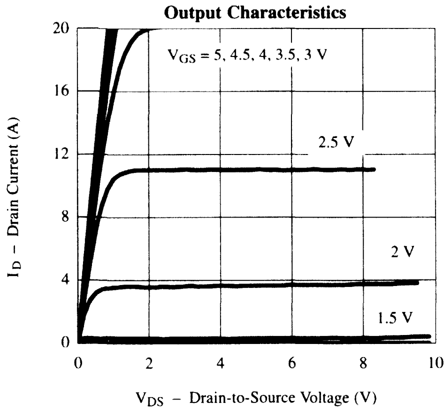
New Product

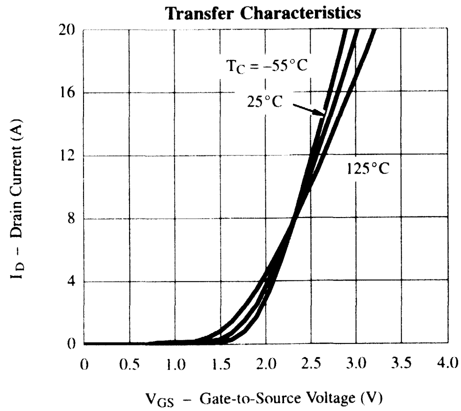
Specifications (T_J = 25°C Unless Otherwise Noted)

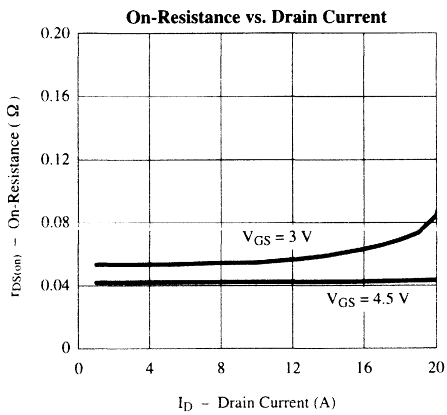
Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Static							
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 µA	N-Ch	0.6			V
		$V_{DS} = V_{GS}$, I_D = –250 µA	P-Ch	–0.6			
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 12 V	N-Ch			± 100	nA
			P-Ch			± 100	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V	N-Ch			1	µA
		V_{DS} = –20 V, V_{GS} = 0 V	P-Ch			–1	
		V_{DS} = 20 V, V_{GS} = 0 V, T_J = 70°C	N-Ch			25	
		V_{DS} = –20 V, V_{GS} = 0 V, T_J = 70°C	P-Ch			–25	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 4.5 V	N-Ch	20			A
		V_{DS} = –5 V, V_{GS} = –4.5 V	P-Ch	–20			
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 4.5 V, I_D = 4.5 A	N-Ch		0.044	0.055	Ω
		V_{GS} = –4.5 V, I_D = 4.0 A	P-Ch		0.064	0.080	
		V_{GS} = 3.0 V, I_D = 3.8 A	N-Ch		0.055	0.075	
		V_{GS} = –3.0 V, I_D = 3.0 A	P-Ch		0.086	0.120	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 4.5 A	N-Ch		11.5		S
		V_{DS} = –15 V, I_D = –4.0 A	P-Ch		9.8		
Diode Forward Voltage[b]	V_{SD}	I_S = 1.7 A, V_{GS} = 0 V	N-Ch		0.73	1.2	V
		I_S = –1.7 A, V_{GS} = 0 V	P-Ch		–0.75	–1.2	
Dynamic[a]							
Total Gate Charge	Q_g	N-Channel V_{DS} = 3.5 V, V_{GS} = 4.5 V, I_D = 0.8 A; P-Channel V_{DS} = –3.5 V, V_{GS} = –4.5 V, I_D = –0.8 A	N-Ch		5.2	10	nC
			P-Ch		7.9	15	
Gate-Source Charge	Q_{gs}		N-Ch		0.95		
			P-Ch		1.60		
Gate-Drain Charge	Q_{gd}		N-Ch		1.15		
			P-Ch		1.90		
Turn-On Delay Time	$t_{d(on)}$	N-Channel V_{DD} = 3.5 V, R_L = 4.3 Ω, I_D ≅ 0.8 A, V_{GEN} = 4.5 V, R_G = 6 Ω; P-Channel V_{DD} = –3.5 V, R_L = 4.3 Ω, I_D ≅ –0.8 A, V_{GEN} = –4.5 V, R_G = 6 Ω	N-Ch		12	20	ns
			P-Ch		20	40	
Rise Time	t_r		N-Ch		22	50	
			P-Ch		52	90	
Turn-Off Delay Time	$t_{d(off)}$		N-Ch		27	50	
			P-Ch		37	60	
Fall Time	t_f		N-Ch		8	20	
			P-Ch		11	20	
Source-Drain Reverse Recovery Time	t_{rr}	N-Channel—I_F = 1.7 A, di/dt = 100 A/µs	N-Ch		60	100	
		P-Channel—I_F = –1.7 A, di/dt = 100 A/µs	P-Ch		60	100	

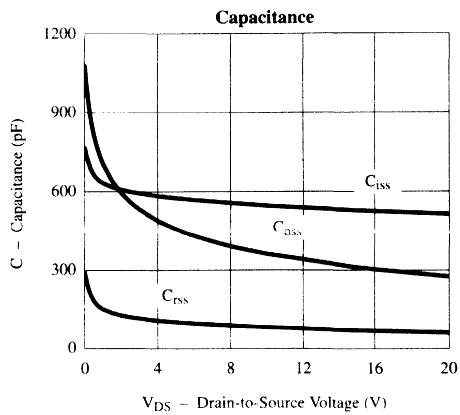
Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

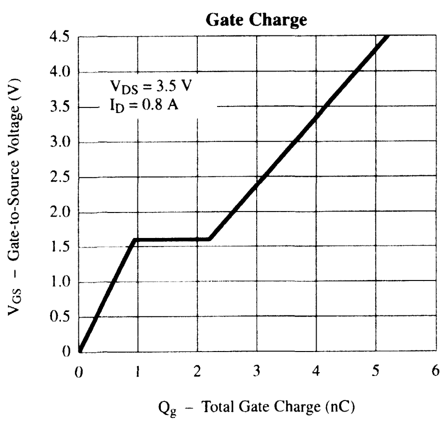
Typical Characteristics (25°C Unless Noted) N-Channel

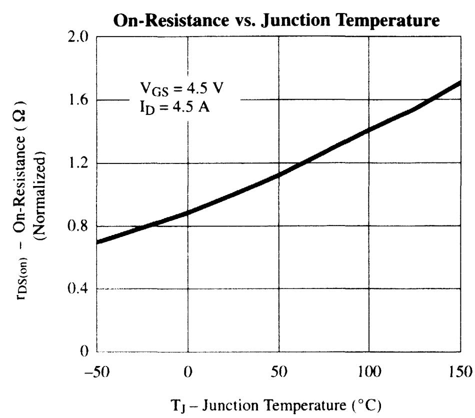






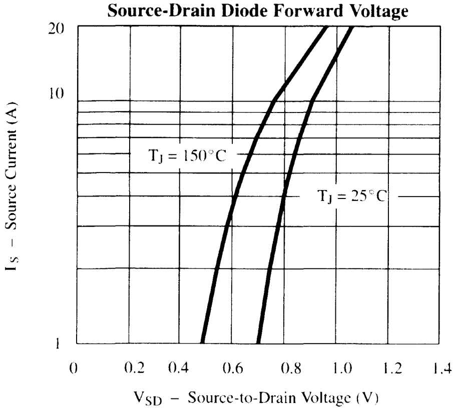


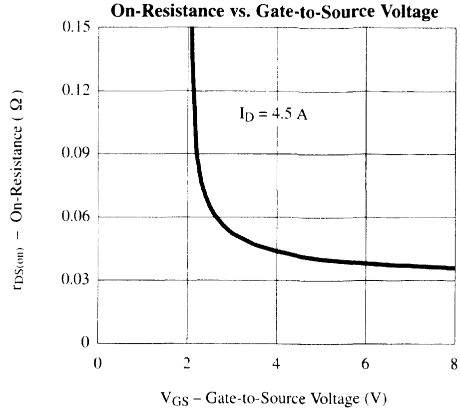


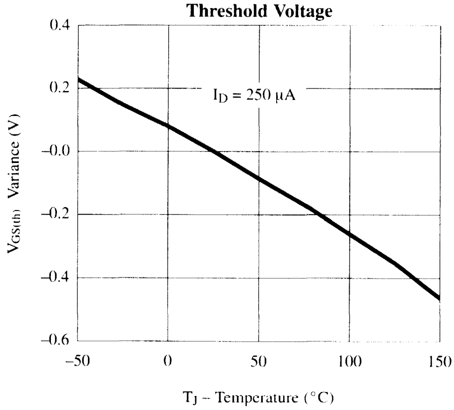


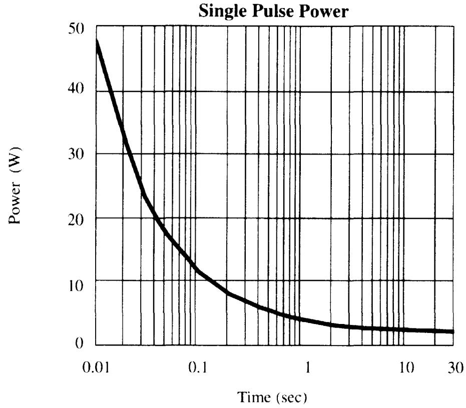
4
High-Efficiency

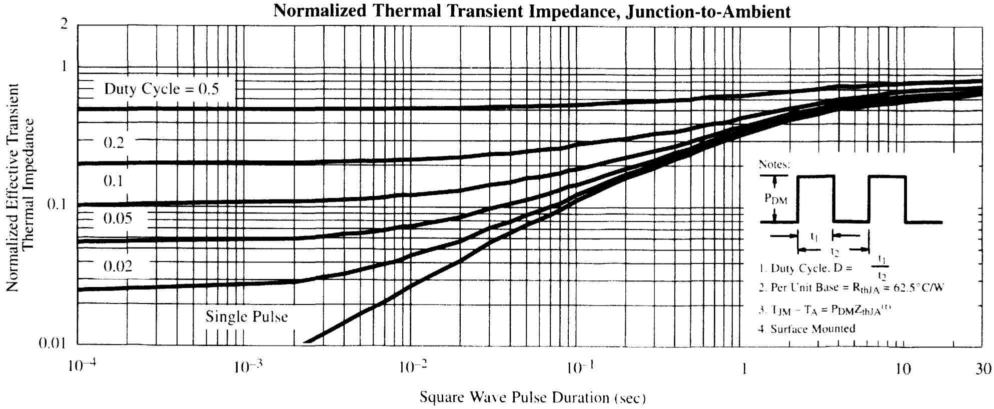
Typical Characteristics (25°C Unless Noted) N-Channel







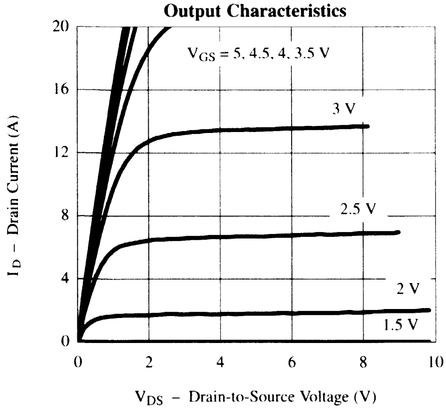




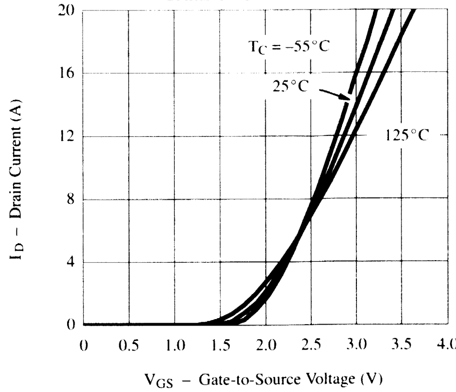
New Product

Typical Characteristics (25°C Unless Noted) P-Channel

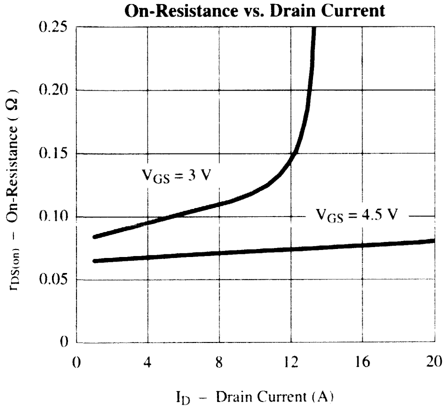
Output Characteristics



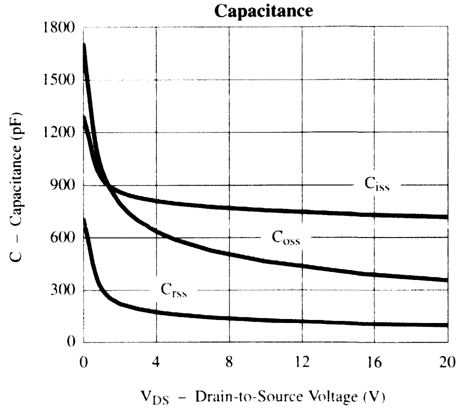
Transfer Characteristics



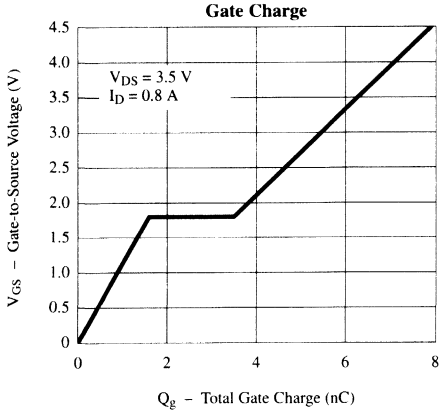
On-Resistance vs. Drain Current



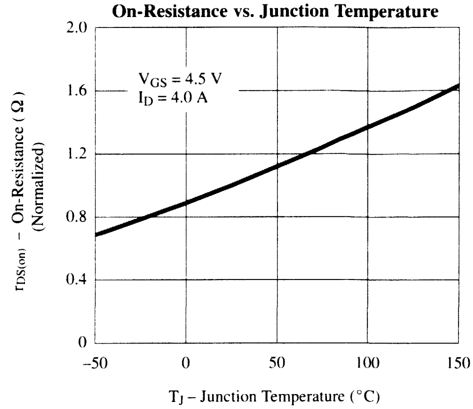
Capacitance



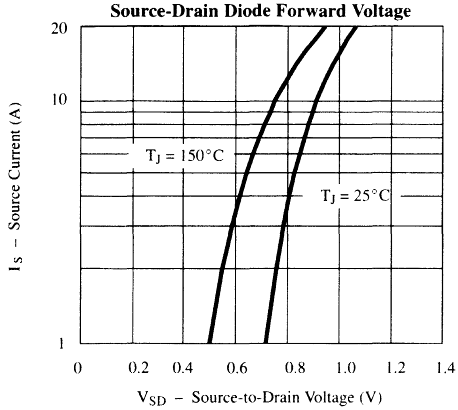
Gate Charge

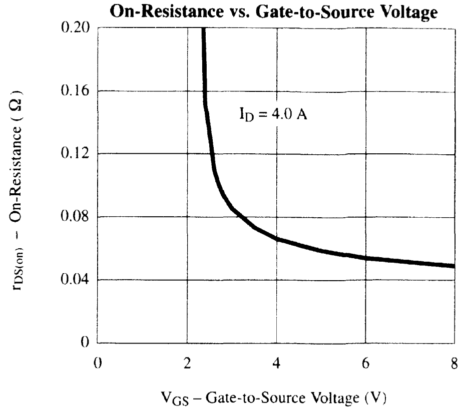


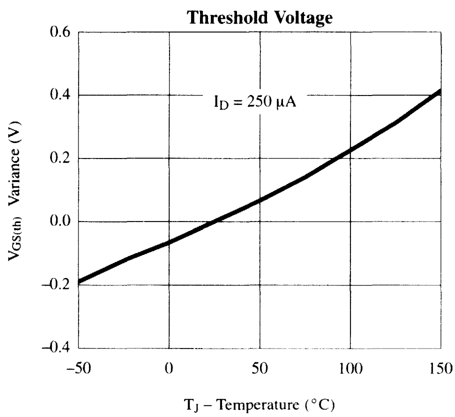
On-Resistance vs. Junction Temperature

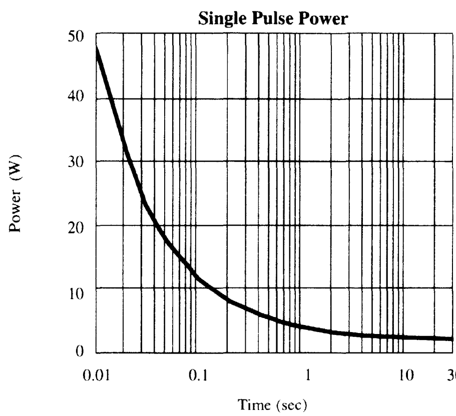


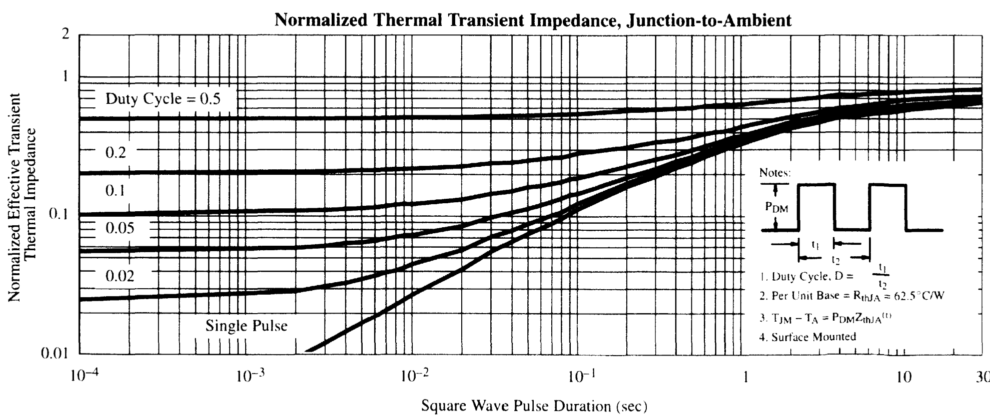
Typical Characteristics (25 °C Unless Noted) P-Channel











New Product

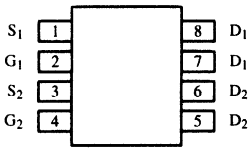
Dual N-Channel Reduced Q_g, Fast Switching MOSFET

Product Summary

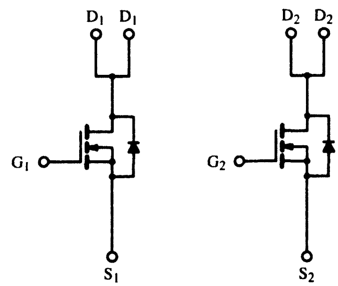
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
20	0.055 @ V_{GS} = 4.5 V	±4.5
	0.075 @ V_{GS} = 3.0 V	±3.8

High-Efficiency
PWM Optimized

SO-8



Top View



N-Channel MOSFET   N-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	± 12	
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	±4.5	A
	T_A = 70°C		±3.6	
Pulsed Drain Current (10 µs Pulse Width)		I_{DM}	±25	
Continuous Source Current (Diode Conduction)[a]		I_S	±1.7	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	2	W
	T_A = 70°C		1.3	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient[a]	R_{thJA}	62.5	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70625.

New Product

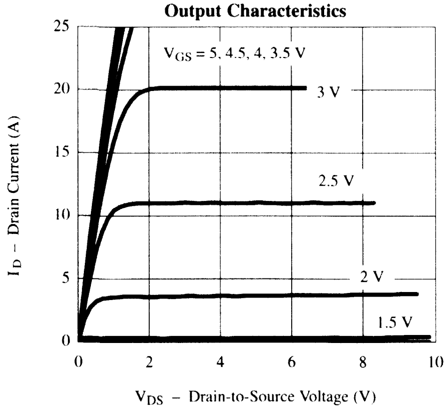
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 µA	0.6			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 12 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V			1	µA
		V_{DS} = 20 V, V_{GS} = 0 V, T_J = 70°C			5	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 5 V	25			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 4.5 V, I_D = 4.5 A		0.044	0.055	Ω
		V_{GS} = 3.0 V, I_D = 3.8 A		0.055	0.075	
Forward Transconductance[b]	g_{fs}	V_{DS} = 10 V, I_D = 4.5 A		11.5		S
Diode Forward Voltage[b]	V_{SD}	I_S = 1.7 A, V_{GS} = 0 V		0.73	1.2	V
Dynamic[a]						
Total Gate Charge	Q_g	V_{DS} = 10 V, V_{GS} = 4.5 V, I_D = 4.5 A		5.5	10	nC
Gate-Source Charge	Q_{gs}			1.2		
Gate-Drain Charge	Q_{gd}			1.5		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 10 V, R_L = 10 Ω I_D ≅ 1 A, V_{GEN} = 4.5 V, R_G = 6 Ω		12	25	ns
Rise Time	t_r			30	60	
Turn-Off Delay Time	$t_{d(off)}$			23	50	
Fall Time	t_f			9	20	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 1.7 A, di/dt = 100 A/µs		60	100	

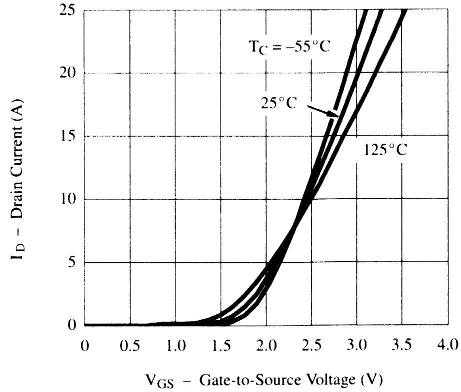
Notes
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

Typical Characteristics (25 °C Unless Otherwise Noted)

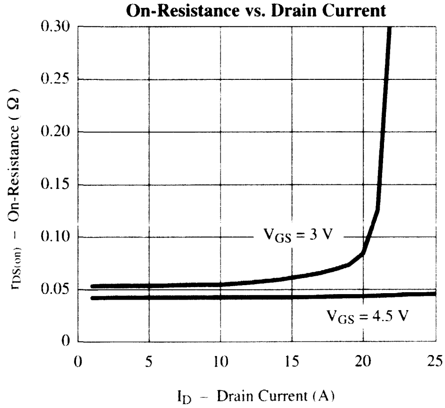
Output Characteristics



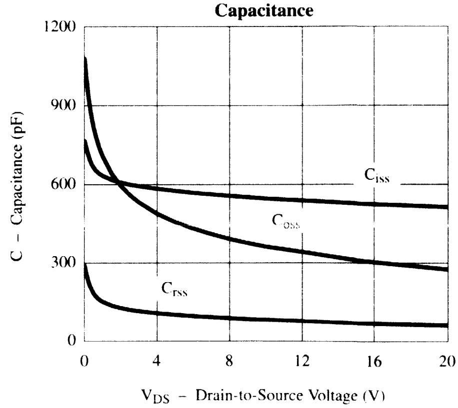
Transfer Characteristics



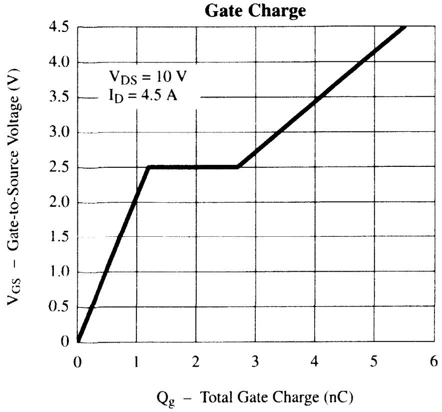
On-Resistance vs. Drain Current



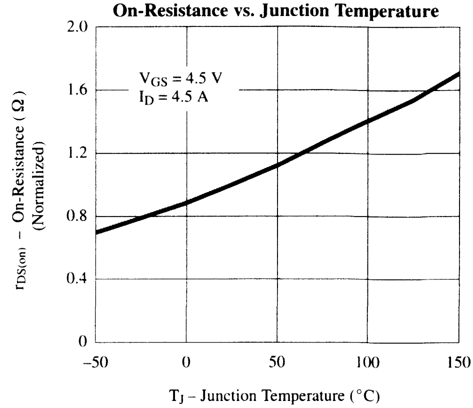
Capacitance



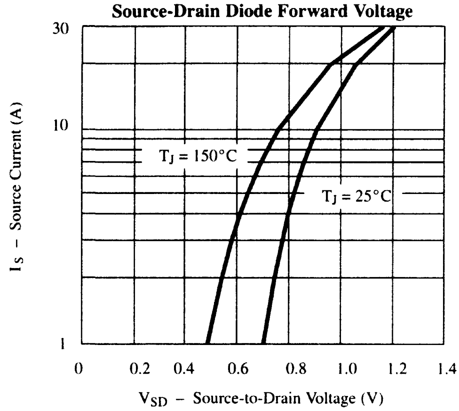
Gate Charge

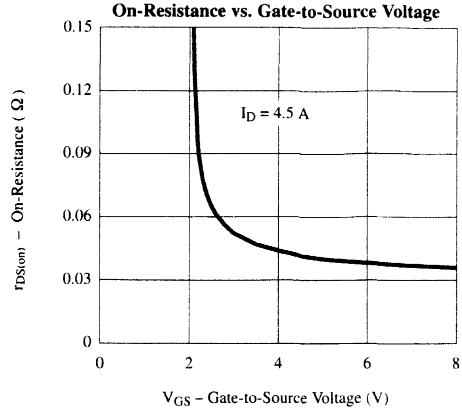


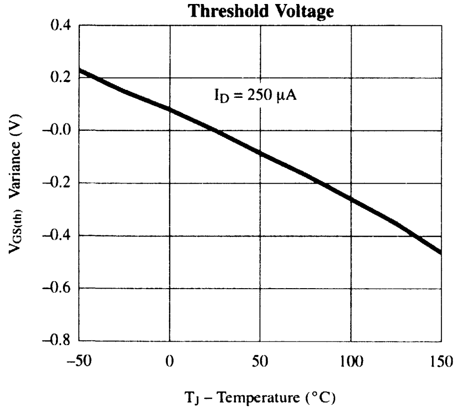
On-Resistance vs. Junction Temperature

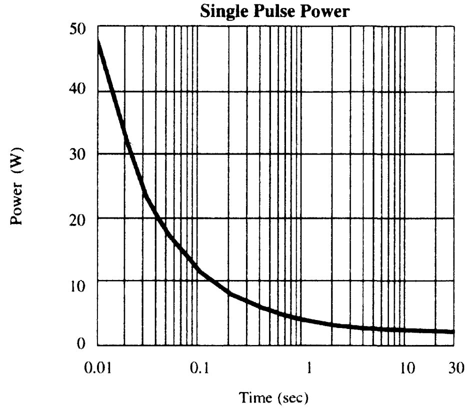


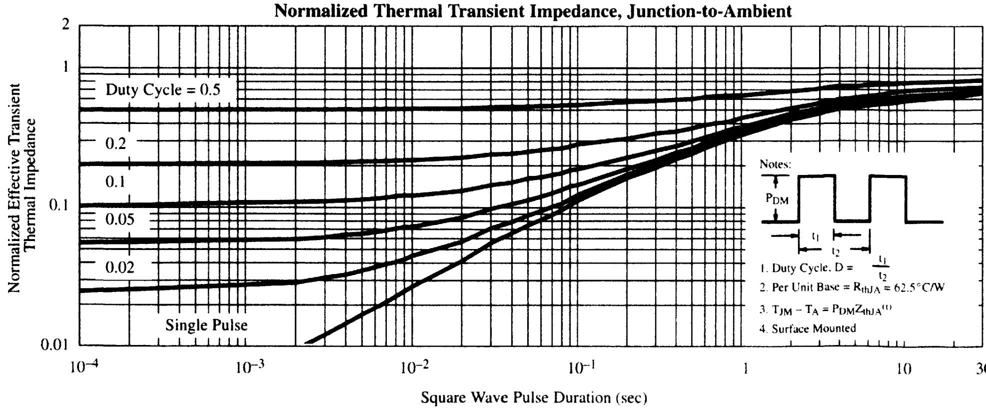
Typical Characteristics (25°C Unless Otherwise Noted)











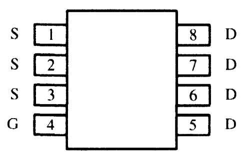
New Product

P-Channel Reduced Q_g, Fast Switching MOSFET

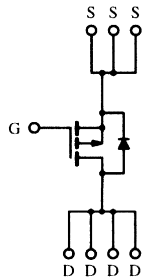
Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
–20	0.040 @ V_{GS} = –4.5 V	±5.9
	0.060 @ V_{GS} = –3.0 V	±4.8

High-Efficiency
PWM Optimized



Top View



P-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	–20	V
Gate-Source Voltage		V_{GS}	± 12	
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	± 5.9	A
	T_A = 70°C		± 4.7	
Pulsed Drain Current		I_{DM}	± 40	
Continuous Source Current (Diode Conduction)[a]		I_S	–2.1	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	2.5	W
	T_A = 70°C		1.6	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient[a]	R_{thJA}	50	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70638.

New Product

Specifications (T_J = 25°C Unless Otherwise Noted)

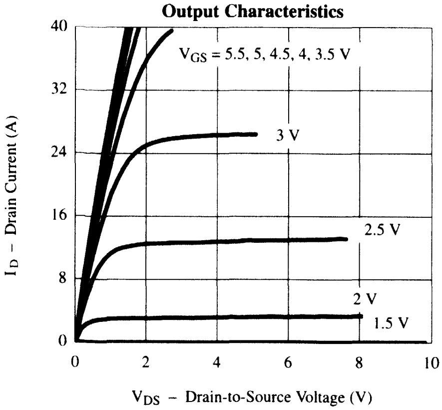
Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250\ \mu A$	–0.6			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = \pm 12$ V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -20$ V, $V_{GS} = 0$ V			-1	µA
		$V_{DS} = -20$ V, $V_{GS} = 0$ V, $T_J = 70°C$			-5	
On-State Drain Current[b]	$I_{D(on)}$	$V_{DS} \leq -5$ V, $V_{GS} = -4.5$ V	–40			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	$V_{GS} = -4.5$ V, $I_D = -5.9$ A		0.033	0.040	Ω
		$V_{GS} = -3.0$ V, $I_D = -2.0$ A		0.044	0.060	
Forward Transconductance[b]	g_{fs}	$V_{DS} = -9$ V, $I_D = -5.9$ A		18		S
Diode Forward Voltage[b]	V_{SD}	$I_S = -2.1$ A, $V_{GS} = 0$ V		–0.75	-1.2	V
Dynamic[a]						
Total Gate Charge	Q_g	$V_{DS} = -10$ V, $V_{GS} = -4.5$ V, $I_D = -5.9$ A		15.8	25	nC
Gate-Source Charge	Q_{gs}			3.0		
Gate-Drain Charge	Q_{gd}			5.4		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10$ V, $R_L = 10\ \Omega$ $I_D \cong -1$ A, $V_{GEN} = -4.5$ V, $R_G = 6\ \Omega$		20	40	ns
Rise Time	t_r			30	60	
Turn-Off Delay Time	$t_{d(off)}$			53	100	
Fall Time	t_f			31	60	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -2.6$, di/dt = 100 A/µs		80	120	

Notes
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

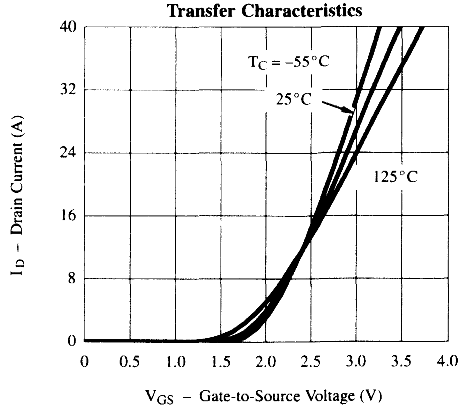
New Product

Typical Characteristics (25°C Unless Otherwise Noted)

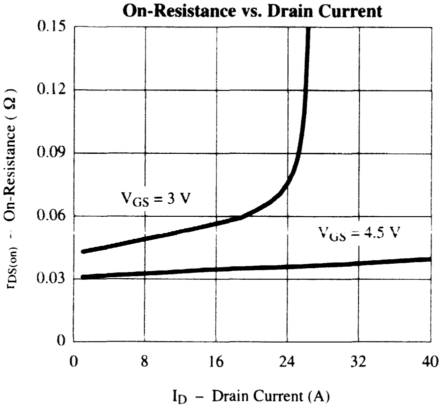
Output Characteristics



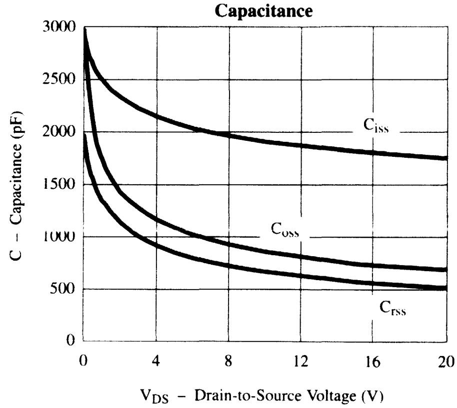
Transfer Characteristics



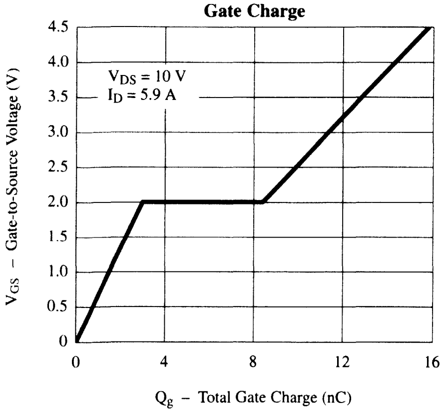
On-Resistance vs. Drain Current



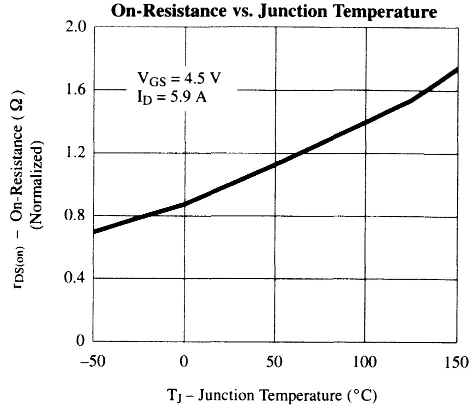
Capacitance



Gate Charge



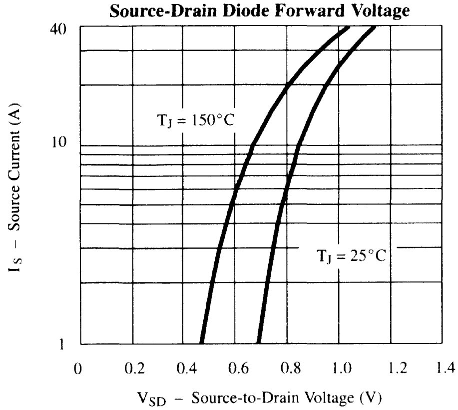
On-Resistance vs. Junction Temperature



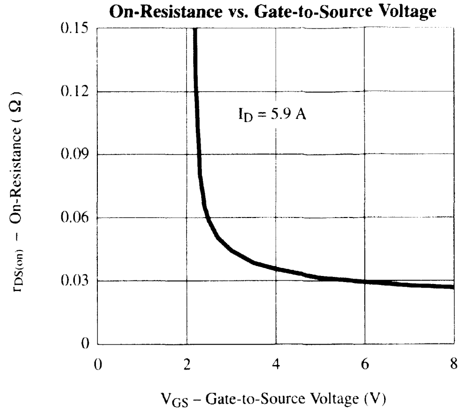
4
High-Efficiency

Typical Characteristics (25 °C Unless Otherwise Noted)

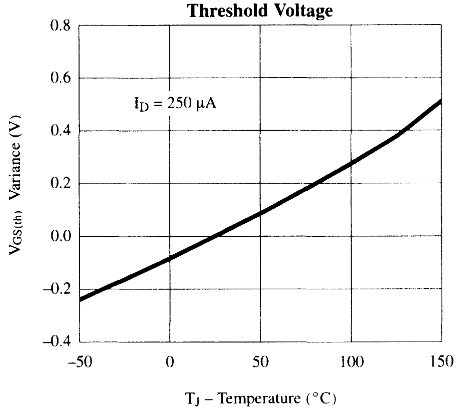
Source-Drain Diode Forward Voltage



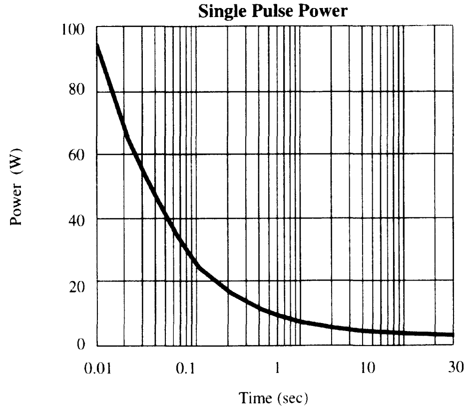
On-Resistance vs. Gate-to-Source Voltage



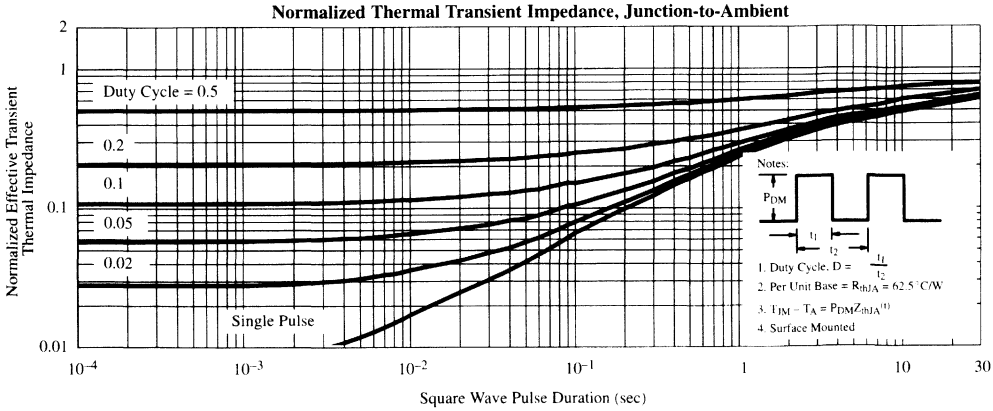
Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient



New Product

Si9804DY

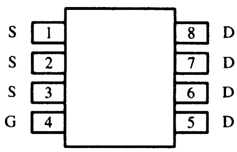
N-Channel Reduced Q_g, Fast Switching MOSFET

Product Summary

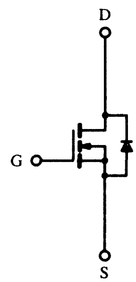
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
20	0.023 @ V_{GS} = 4.5 V	± 7.8
	0.030 @ V_{GS} = 3.0 V	± 6.8

High-Efficiency
PWM Optimized

SO-8



Top View



N-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	± 12	
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	± 7.8	A
	T_A = 70°C		± 6.2	
Pulsed Drain Current (10 µs Pulse Width)		I_{DM}	± 40	
Continuous Source Current (Diode Conduction)[a]		I_S	± 2.1	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	2.5	W
	T_A = 70°C		1.6	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient[a]	R_{thJA}	50	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 10 sec.

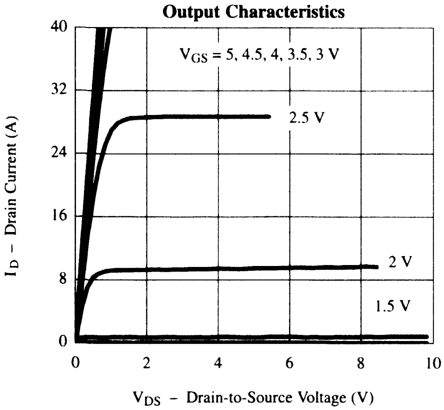
Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70626.

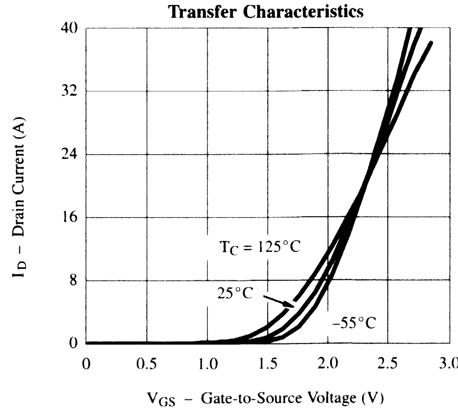
Specifications (T_J = 25°C Unless Otherwise Noted)

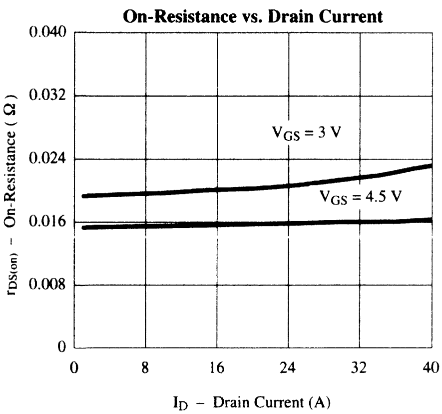
Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 µA	0.6			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 12 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V			1	µA
		V_{DS} = 20 V, V_{GS} = 0 V, T_J = 55°C			5	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 4.5 V	40			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 4.5 V, I_D = 7.8 A		0.018	0.023	Ω
		V_{GS} = 3.0 V, I_D = 6.8 A		0.022	0.030	
Forward Transconductance[b]	g_{fs}	V_{DS} = 10 V, I_D = 7.8 A		25		S
Diode Forward Voltage[b]	V_{SD}	I_S = 2.1 A, V_{GS} = 0 V		0.71	1.2	V
Dynamic[a]						
Total Gate Charge	Q_g	V_{DS} = 10 V, V_{GS} = 4.5 V, I_D = 7.8 A		13.5	20	nC
Gate-Source Charge	Q_{gs}			2.4		
Gate-Drain Charge	Q_{gd}			4.2		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 10 V, R_L = 10 Ω I_D ≅ 1 A, V_{GEN} = 4.5 V, R_G = 6 Ω		16	30	ns
Rise Time	t_r			30	60	
Turn-Off Delay Time	$t_{d(off)}$			46	90	
Fall Time	t_f			18	35	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 2.1 A, di/dt = 100 A/µs		80	120	

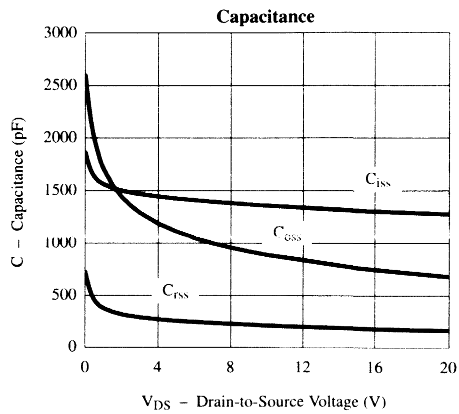
Notes
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

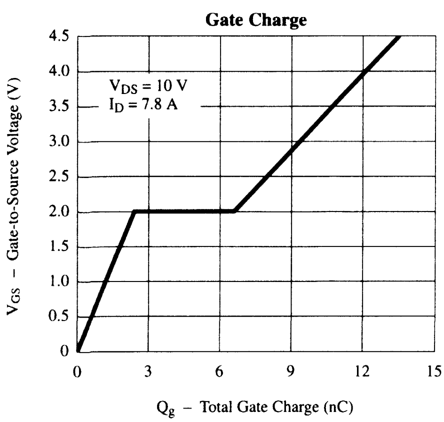
Typical Characteristics (25°C Unless Otherwise Noted)

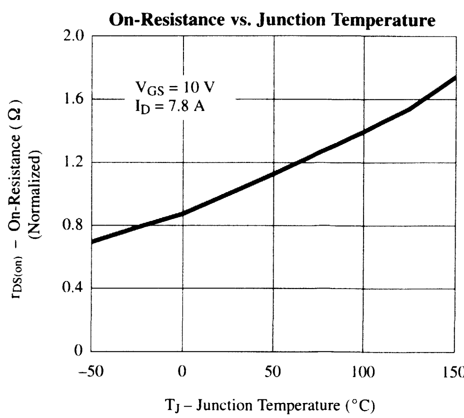






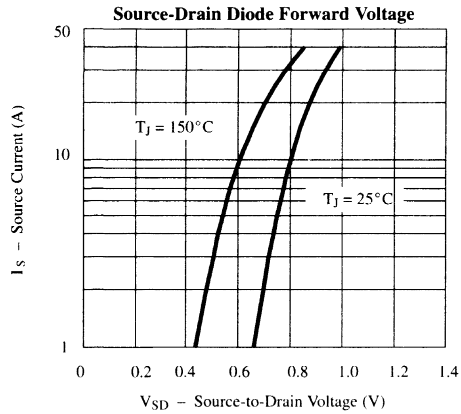


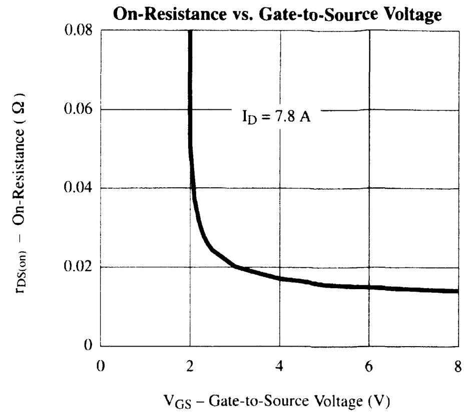


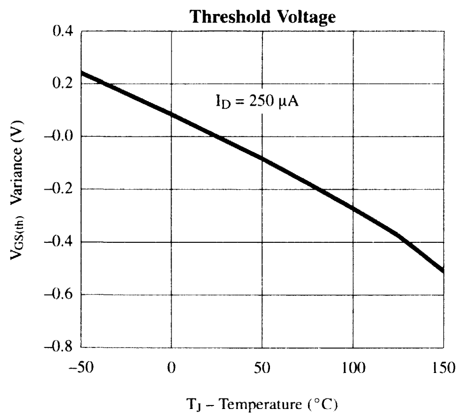


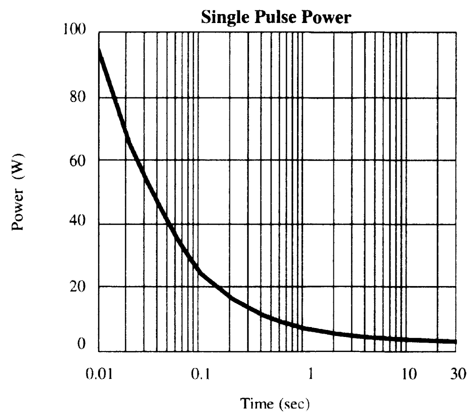
New Product

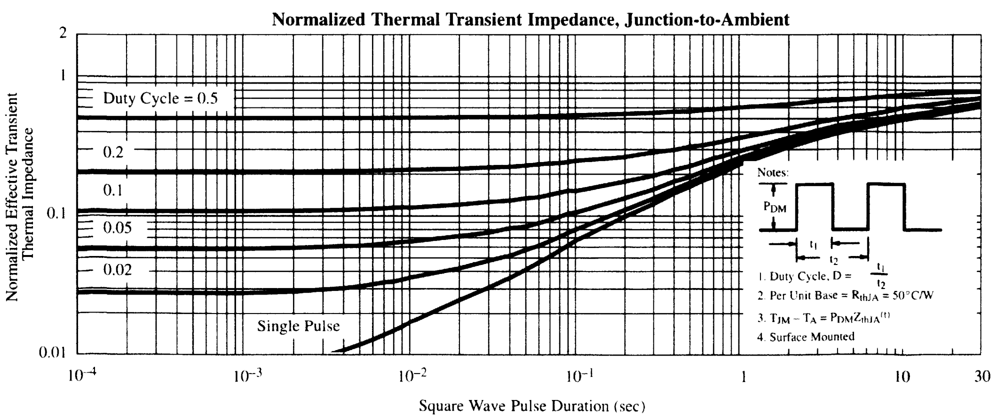
Typical Characteristics (25°C Unless Otherwise Noted)











1 **How FaxBack Works**

If you're calling for the first time, please follow these easy steps.

ABC 2 **From a Touch-Tone Phone, Just Dial 1-408-970-5600**

FaxBack will answer and lead you through a series of easy-to-understand automated voice prompts.

Order A Directory

You will be asked whether you want to order a directory. Please order any or all of the directories listed below. A directory describes the available documents and gives you the FaxBack order numbers for those documents.

DEF 3 **Enter Your Fax Number**

When you have finished ordering, and following the prompt, type in the area code and phone number on your touch-tone phone. If you are sending the information to a fax machine outside of North America, make sure you dial "011" first.

GHI 4 **Identify Your Fax**

FaxBack lets you choose how your documents will be addressed. You can enter your name or your phone number. Just follow this simple system.

To enter a letter, press its key 1, 2, or 3 times: 2 enters **A**; 2 2 enters **B**; 2 2 2 enters **C**.

Special characters: 1 1 — **Q**; 1 1 1 — **Z**; # # — **SPACE**.

To back up and correct a letter, press: *. To end, press: #. For complete instructions, press: 0.

The documents you request will be sent with a cover sheet bearing your name or addressed to your direct phone number.

JKL 5 **Hang Up**

The information you ordered will be sent immediately. It's as easy as 1 + 2 = 3!

Once you have received and reviewed your directories, just call back and enter the Siliconix FaxBack numbers of the documents you wish to request.

In most cases, you will receive your documents within 5-10 minutes. If your fax machine is in use when FaxBack is ready to send your documents, FaxBack will automatically call back – up to three times (at two minute intervals) – until it reaches your fax machine. If after the third call your machine is still in use, you will have to call back and order your documents again.

The following literature is designed to help you use Siliconix products in your applications. Call our FaxBack system (1-408-970-5600) to have the document sent to you immediately via facsimile, or to order a copy to be sent by mail, call 1-800-554-5565.

To request additional literature, please call your local TEMIC Sales Representative. Office listings with phone and fax numbers are available in the Sales Offices section of this data book.

Application Notes for Siliconix Power Products

Application Note Number	FaxBack Number	Description
LITTLE FOOT® MOSFETs		
AN801	70591	**Designing with Complementary Power MOSFETs in Surface-Mount (SO-8) Packages** The LITTLE FOOT complementary n- and p-channel Si9942DY can be used to drive inductive loads such as motors, solenoids, and relays directly, or it may be used as a low-impedance buffer to drive larger power MOSFETs or capacitive loads. In 12-V battery-powered applications, the Si9942DY allows a substantial increase in motor size without the need for additional heatsinking.
AN802	70592	**Low-Voltage Motor Drive Designs Using N-Channel Dual MOSFETS in Surface-Mount Packages** Dual n-channel LITTLE FOOT devices offer on-resistance advantages which extend the power range of surface-mount power devices. With the selection of a high-side gate drive circuit that complements an application's needs, an n-channel half-bridge can provide a surface-mount option that is economical and reliable.
AN803	70593	**Thermal Characteristics of Siliconix's LITTLE FOOT Family of Surface-Mount MOSFETs** Siliconix' LITTLE FOOT family of surface-mount power MOSFETs provides improved thermal transfer characteristics, high current handling capability, and lower on-resistance compared with DPAK and SOT packages. The copper lead frames designed for the LITTLE FOOT family maximize heat transfer to the PC board. Combined with Siliconix' high-density transistor technologies, the result is a significantly extended range for surface-mount devices in power applications.
AN1001	70571	**LITE FOOT, The Next Step in Surface-Mount Power MOSFETs** LITE FOOT is the first family of power MOSFETs combining high-density n- and p-channel technologies with TSSOP packaging. With a 1.1 mm profile, LITE FOOT devices are small enough to fit into any standard PC Card (PCMCIA) card. They provide an equally compact solution for load switching in small form-factor disk drives, cellular telephones, notebook computers, PDAs, and other applications where space and battery life is at a premium.
Power MOSFETs		
AN601	70572	**Unclamped Inductive Switching Rugged MOSFETs for Rugged Environments** This application note reviews the history of unclamped inductive switching (UIS) and examines various theories pertaining to failure. It further identifies what appears to be two releated mechanisms -- thermal and bipolar -- believed to be responsible for failure during UIS and concludes by recommending how a power MOSFET should be qualified for ruggedness in the data sheet.
AN603	70573	**Designing With the Si9978DW Configurable H-Bridge Controller** The Si9978DW monolithic controller confronts issues common to bipolar and MOS technology parts. Separating the controller from the MOSFETs assures flexible current handling, small size and ease of assembly. The Si9978DW is designed to be used with LITTLE FOOT MOSFETs to create an all-n-channel H-bridge or two separate half bridges. The dual function allows flexibility, standardization of components and reduced inventory costs. Features are an integral high-side drive circuitry and an internal voltage regulator, which allows operation over a 20- to 40-V dc input voltage range. Protection features include cross-conduction protection and current limiting. The $\overline{\text{FAULT}}$ outputs indicate undervoltage lockout or overcurrent shutdown.
AN805	70649	**Power MOSFETs Optimized for Low-Voltage DC/DC Conversion** Designers of low-voltage dc-to-dc converters have two main concerns: reducing size and reducing losses. As a way of reducing size, designers are increasing switching frequencies. But the result has often been reduced converter efficiency. To minimize losses, MOSFET manufacturers have generally focused on lowering on-resistance. But the results have not been optimal for dc-to-dc conversion designs, since gate charge and switching speed issues have been largely ignored. The dominant losses associated with MOSFETs were once conduction losses, but this is no longer the case.

Application Notes for Siliconix Power Products (Cont'd)

Application Note Number	FaxBack Number	Description
Power ICs		
AN701	**70575**	**Designing High-Frequency DC-to-DC Converters with the Si9114 Switchmode Controller** The Si9114 controller enables high-frequency power conversion by reducing delay times and adding additional features over previous generation products. As a result, dc-to-dc converters can be designed for frequencies up to 1 MHz with simple PWM topologies instead of the complex resonant ones. High-frequency designs with the Si9114 will enable designers to reduce the size of energy storage components, increase reliability by using ceramic capacitors, and simplify the implementation of a distributed power architecture.
AN702	**70576**	**Efficient ISDN Power Converters Using the Si9100** The Si9100 power IC facilitates compliance with ISDN design requirements with a minimum number of external parts. To illustrate this capability, a discontinuous conduction mode (DCM) flyback converter was built and tested with measured efficiency greater than 80% for a wide range of loads.
AN703	**70577**	**Designing DC/DC Converters with the Si9110 Switchmode Controller** Si9110 is the first BiC/DMOS switchmode controller IC to provide switching frequencies in the 100- to 500-kHz range while keeping current limit delay time under approximately 100 ns. To illustrate the Si9110's capabilities, a 15-W forward converter is presented, providing 5-V and 12-V outputs from a 9- to 36-V input range.
AN704	**70578**	**Designing DC/DC Converters to Meet CCITT Specifications for ISDN Terminals** This application note specifically addresses design issues relating to emergency-designated ISDN terminals and presents design details for a dc-to-dc converter which conforms to the international standard.
AN705	**70579**	**The Si9910 Adaptive Power MOSFET Driver Improves Performance in High-Voltage Half-Bridge Applications** The Si9910DY introduces a new generation of "adaptive" power MOSFET gate drivers that use active feedback to protect the power MOSFET, while allowing logic-level control of high-voltage signals. When all of its protective options are enabled, the Si9910DY is capable of controlling the power MOSFET dv/dt, maximum peak current, minimum gate-drive voltage, and maximum source-drain voltage drop.
AN707	**70580**	**Designing Low-Power Off-Line Flyback Converters Using the Si9120 Switchmode Controller IC** The Si9120 was designed to get high efficiency from low-power off-line power supplies. This current-mode control PWM IC reduces typical quiescent power requirements to 0.85 mA while driving a 500-pF load at 50 kHz. The chip contains MOS capacitors for the clock circuit, so the only external timing component required is a resistor to set the operating frequency.
AN708	**70581**	**Low-Power Universal-Input Power Supply Achieves High Efficiency** A flyback circuit using the Si9120 PWM controller demonstrates that designing universal-input supplies can be a simple task. Good regulation is achieved while maintaining the 3750-V ac input-to-output isolation mandated by VDE. The Si9120 eliminates the need for external start-up circuitry, and its foldback current limiting requires no feedback across the isolation boundary.
AN709	**70582**	**Designing with the Si9976DY N-Channel Half-Bridge Driver and LITTLE FOOT Dual MOSFETs** The combination of the Si9976DY and a LITTLE FOOT MOSFET rated between 2 and 5 A creates a powerful and flexible solution for power switching in dc motor drives in 20- to 40-V systems.
AN710	**70583**	**High-Efficiency Buck Converter for Notebook Computers** This application note presents a dc-to-dc converter consisting of the Si9150CY BiCMOS controller IC and LITTLE FOOT low-voltage MOSFETs. In notebook computers and other portable products, the converter achieves a maximum efficiency of 94% while producing 400 mA at 3.3 V with input voltage of 6 V. The low losses of this efficient buck converter eliminate the need for heavy heat sinks and device packaging, and makes energy that is normally consumed by the power converter available for the application.
AN713	**70584**	**A 1-Watt Flyback Converter Using the Si9100** Power integrated circuit technology allows low-power CMOS control circuits to be combined with DMOS power transistors in the Si9100. The resulting reduction in parts count decreases system cost, improves reliability, and simplifies circuit design in feature phones and ISDN terminals.

Application Notes for Siliconix Power Products (Cont'd)

Application Note Number	FaxBack Number	Description
Power ICs		
AN714	70585	**A Compact Controller for Brushless DC Motors** The Si9979 is a monolithic controller with integral high-side drive circuitry, allowing easy implementation of an all-n-channel three-phase bridge. An internal voltage regulator allows the Si9979 to operate over a wide input voltage range, 20 to 40 V DC, and to power commutation sensors over this same range. Housed in a 7 mm SQFP package, the Si9979 reduces assembly cost and simplifies both motor and electronics packaging.
AN715	70586	**Designing Low-Voltage DC/DC Converters with the Si9145** The Si9145 switchmode controller IC is designed to make dc-to-dc conversion smaller and more efficient in low-voltage, low-power applications such as portable cellular phones and other battery-operated equipment. This small-outline device has been configured so that the most popular conventional topologies, including buck, synchronous buck, and boost can be easily implemented.
AN716	70587	**Designing with Siliconix PC Card (PCMCIA) Power Interface Switches** Siliconix offers a series of integrated power MOSFETs specifically designed for the strict demands of the PC Card power interface. The Si97XX series includes devices supporting one and two PC Card slots in battery-operated notebook, subnotebook, and palmtop computers.
AN718	70588	**Powering the Pentium™ VRE with the Si9145 Voltage Mode Controlled PWM Converter** Built on a leading-edge CBiC/D process, Siliconix' Si9145BY is the only voltage-mode controlled PWM IC capable of switching up to 2 MHz and providing a 25-MHz error amplifier. Its 100-kHz closed-loop bandwidth switching converter meets the dynamic switching transient requirements of the Pentium microprocessor without the need for numerous output capacitors.
AN719	70589	**Using the Si9145 PWM Converter with the Pentium™ P55 and P6 Microprocessors** Although the P55 and P6 Pentium microprocessors push the limits of switching power supplies, the Si9145 PWM controller IC meets their demanding requirements with switching speeds of 400 kHz and a 25-MHz error amplifier to generate a 100-kHz closed-loop converter bandwidth.
AN720	70590	**Si9986CY Buffered H-Bridge** The Si9986CY is a buffered H-bridge that will eliminate all the external discretes that are normally needed to prevent shoot-through in low-voltage brushed motor, stepper motor, and actuator applications.

LITTLE FOOT Family of Power MOSFETs

Introduction

Reliability at Siliconix is ensured by two primary programs: the Reliability Qualification Program and the Reliability Monitoring Program. Siliconix publishes this data by product family and it can be obtained by request through your local sales office.

Qualification Program

Qualification programs of accelerated stress testing are developed for the introduction of new devices (die qualifications), packages, major process changes, new materials or suppliers, new manufacturing equipment, and new manufacturing locations.

A qualification starts after a qualification test plan is developed. This plan specifies the following:

- Purpose and scope
- Device or geometry types and packages being qualified
- Process and assembly specs involved
- Test vehicles and location
- Tests and stresses
- Duration of each stress
- Sample sizes
- Acceptance criteria
- Number of lots required

Monitoring Program

The Reliability Monitoring Program, which includes accelerated life tests, is designed to continuously monitor product reliability. The program furnishes up-to-date failure-rate and failure-mechanism data which can be used to predict and improve long-term reliability performance. The Monitoring Program covers a wide range of technologies and product lines manufactured by Siliconix. In order to accomplish this, products are grouped by similar technologies. For example, components built in the same wafer fab, using the same manufacturing processes, having similar complexity, functionality, and package types are grouped into a technology family. One component or more representing each technology group is monitored according to a quarterly schedule. An internal Reliability Performance Monitor report is issued every period and is reviewed by all engineering groups to assure improvement of product reliability.

Accelerated Reliability Tests Used

Accelerated tests were developed to shorten the time required for reliability testing. The life cycle of a component is accelerated by applying stress that is more severe than that encountered under normal operating conditions. This acceleration is produced by elevating temperatures, increasing humidity or pressure, alternating hot and cold temperature, switching power on and off, or some combination of these conditions. The test results are used to predict normal operating performance. In the sections below we present a brief description of each stress, together with the results for each tested lot.

Summary of Tests

High-Temperature Reverse-Bias (HTRB) Test

The HTRB accelerated test is performed under reverse biasing at an elevated temperature of 150°C or 175°C with the drain-to-source junction reversed biased to 80% of BV_{DSS}. According to the reliability monitor specification, devices are to be tested at 168 hours (providing a fast reaction and infant mortality indication) and at the end point of 1000 hours. Reliability failure rates (expressed in FITs) are then calculated from the long-term results. The reverse-biased test condition checks the integrity of the field termination and the quality of the body-drain junction. This test also detects surface states, especially in the termination area.

Long-Term Reliability (FIT) Rate for HTRB*

Number of Units	Equivalent Device Hours at 55°C and 0.6 eV	FITs at 60% CL
24,216	1,037,357,428	0.877

*Two year window on test results, January 1995 to December 1996.

High-Temperature Gate-Bias (HTGB) Test

The HTGB accelerated test is performed with the gate biased to 80% of the gate-to-source voltage rating and at an elevated temperature of 150°C. Test points are the same as for the HTRB stress. Biasing of the gate accelerates failures due to oxide defects or the presence of mobile ions. The long-term results are used in the prediction of reliability failures.

Long-Term Reliability (FIT) Rate HTGB Stress*

Number of Units	Equivalent Device Hours at 55°C and 0.6 eV	FITs at 60% CL
24,218	1,042,024,953	0.873

Temperature Cycling Test

Temperature cycling exploits the differences in thermal coefficients of expansion between silicon and the other materials used in die fabrication and packaging. Each cycle consists of 10-minute exposures at –65°C and 150°C with a 1-minute transfer at room temperature between the temperature extremes. This test reveals potential weaknesses in die and package materials and construction and in the integration of the die and package.

Temperature Cycling Test*

Total Device Cycles	Failures
5,625,000	0

Thermal Shock Test

The purpose of the thermal shock test is similar to that of temperature cycling. This stress is more extreme, however, due to the fact that the ambient medium is liquid and not air, and the transition time is much shorter than for temperature cycling.

Each cycle consists of a 5-minute exposure at –65°C and 150°C with a maximum 10-second transfer time between the temperature extremes.

Thermal Shock Test*

Total Device Cycles	Failures
630,000	0

Bias Humidity Test

The bias humidity test is used to test plastic packaged devices for the effects of moisture penetration while electrical potentials are applied. The components are placed in an HTRB-biased condition and then are subjected for 1000 hours to a temperature of 85°C and a relative humidity 85%. This test confirms package integrity.

STRESS: Biased Humidity Test*

Total Device Hours	Failures
3,966,500	0

Pressure Pot Test

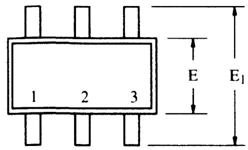
In the pressure pot test, water vapor is forced into non-hermetic packages via micro gaps in the package-lead seal. Water is then carried to the die surface via capillary action of the bond wires. Electrical leakage may result. External contamination of the package or lead finish may be transported to the die or may directly cause corrosion of the leads.

Pressure Pot Test*

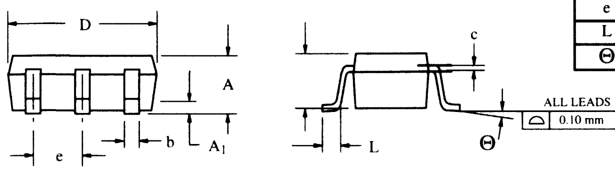
Total Device Hours	Failures
939,072	0

*Two year window on test results, January 1995 to December 1996.

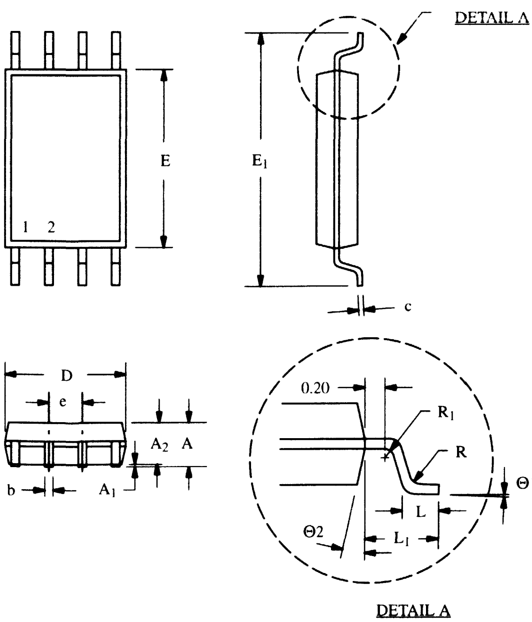
TSOP Package, 6-Pin



Dim	Millimeters Min	Millimeters Max	Inches Min	Inches Max
A	–	1.10	–	0.043
A_1	0.01	0.10	0.0004	0.004
b	0.25	0.50	0.010	0.020
c	0.10	0.26	0.004	0.010
D	2.90	3.10	0.114	0.122
E	1.30	1.70	0.051	0.067
E_1	2.75 BSC		0.108 BSC	
e	1.00 BSC		0.039 BSC	
L	0.20	0.60	0.008	0.024
Θ	0°	8°	0°	8°

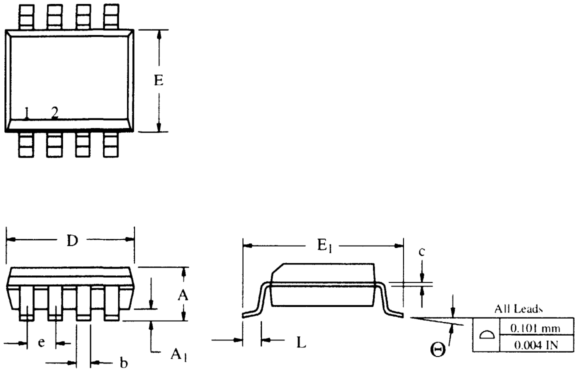


TSSOP Package, 8- and 28-Pin



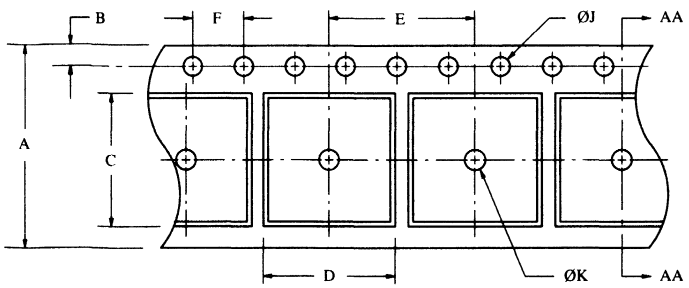
Dim	Millimeters Min	Millimeters Max	Inches Min	Inches Max
A	1.05	1.20	0.041	0.047
A_1	0.05	0.15	0.002	0.006
A_2	–	1.05	–	0.041
b	0.25	0.30	0.010	0.012
c	0.127		0.005	
D-8	2.90	3.10	0.114	0.122
D-28	9.60	9.80	0.378	0.386
E	4.30	4.50	0.170	0.177
E_1	6.20	6.60	0.244	0.260
e	0.65 BSC		0.025 BSC	
L	0.50	0.70	0.020	0.028
L_1	1.0		0.039	
R	0.09	–	0.004	–
R_1	0.09	–	0.004	–
Θ1	0°	8°	0°	8°
Θ2	12°			

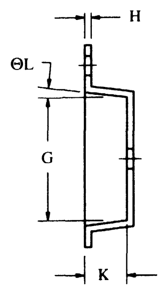
■ SO Package, 8- to 16-Pin



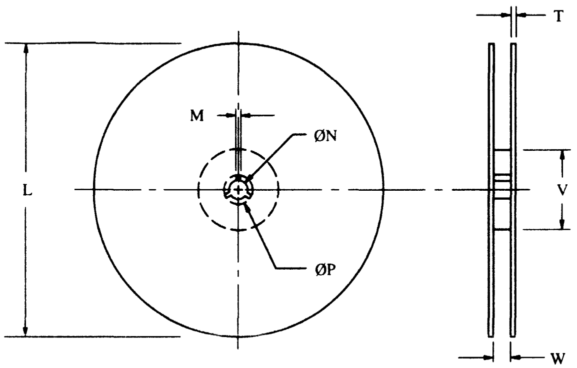
Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.20	0.004	0.008
B	0.35	0.45	0.014	0.018
c	0.18	0.23	0.007	0.009
D-8	4.69	5.00	0.185	0.196
D-14	8.55	8.75	0.336	0.344
D-16	9.80	10.00	0.385	0.393
E	3.50	4.05	0.140	0.160
E_1	5.70	6.30	0.224	0.248
e	1.27 BSC		0.050 BSC	
L	0.60	0.80	0.024	0.031
Θ	0°	8°	0°	8°

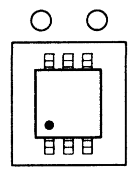
■ Tape and Reel Options for TSOP-6





SECTION A-A



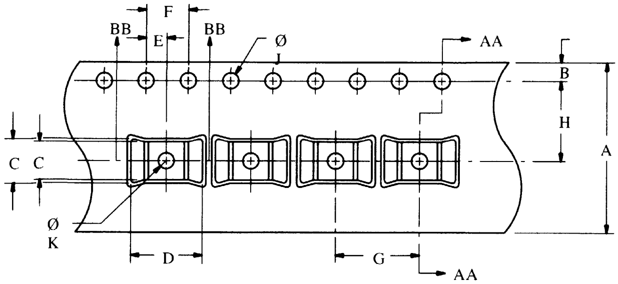


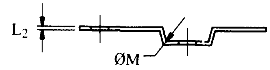
Package Orientation

Quantity Per Reel		
Device	**Reel Size**	**Quantity**
Si34xxDX-T1	7-inches	3,000
Si34xxDX-T2	7-inches	500
Si34xxDX-T3	13-inches	10,000

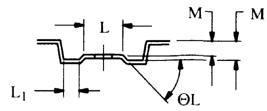
	T1				T3			
	Millimeters		Inches		Millimeters		Inches	
Dim	Min	Max	Min	Max	Min	Max	Min	Max
A	7.70	8.30	0.303	0.327	7.70	8.30	0.303	0.327
B	1.65	1.85	0.065	0.073	1.65	1.85	0.065	0.073
C	3.10	3.30	0.122	0.130	3.10	3.30	0.122	0.130
D	3.05	3.25	0.120	0.128	3.05	3.25	0.120	0.128
E	3.90	4.10	0.154	0.161	3.90	4.10	0.154	0.161
F	3.90	4.10	0.154	0.161	3.90	4.10	0.154	0.161
G	3.10	3.30	0.122	0.130	3.10	3.30	0.122	0.130
H	0.17	0.23	0.007	0.009	0.17	0.23	0.007	0.009
ØJ	1.50	1.60	0.059	0.063	1.50	1.60	0.059	0.063
K	1.30	1.50	0.051	0.059	1.30	1.50	0.051	0.059
ØK	1.00	1.10	0.039	0.043	1.00	1.10	0.039	0.043
L	170	180	6.929	7.087	328	332	12.91	13.07
ΘL	–	3°	–	3°	–	3°	–	3°
M	1.50	2.50	0.059	0.098	1.50	2.50	0.059	0.098
ØN	12.8	13.2	0.504	0.520	12.8	13.2	0.504	0.520
ØP	21.5	22.5	0.846	0.886	21.5	22.5	0.847	0.886
T	1.00	2.00	0.039	0.078	1.00	2.00	0.039	0.078
V	53.0	54.0	2.087	2.126	53.0	54.0	2.087	2.126
W	7.90	8.90	0.311	0.350	24.4	16.4	0.961	1.039

Tape and Reel Options for TSSOP-8 and TSSOP-28

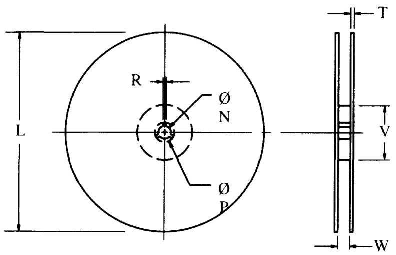




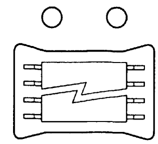
SECTION AA



SECTION BB



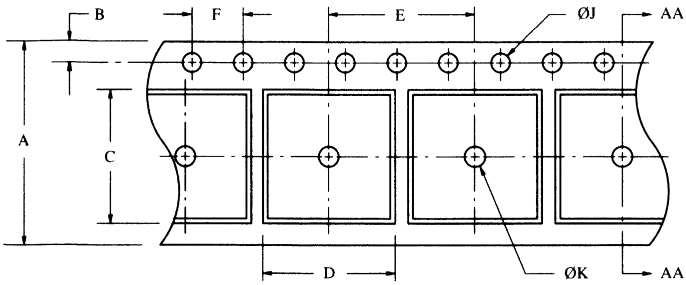
Quantity Per Reel	
TSSOP-8	3000
TSSOP-28	3000

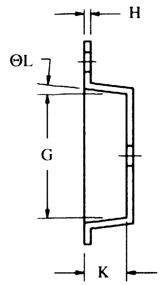


Package Orientation

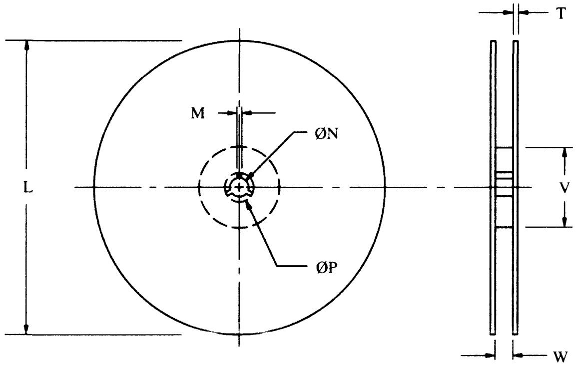
	TSSOP-8				TSSOP-28			
	Millimeters		Inches		Millimeters		Inches	
Dim	Min	Max	Min	Max	Min	Max	Min	Max
A	15.70	16.30	0.618	0.641	15.70	16.30	0.618	0.641
B	1.65	1.85	0.065	0.073	1.65	1.85	0.065	0.073
C	3.50	3.70	0.138	0.146	10.1	10.3	0.398	0.406
C_1	4.20	4.40	0.165	0.173	10.3	11.0	0.425	0.433
D	6.80	7.00	0.268	0.276	6.80	7.00	0.268	0.276
E	1.95	2.05	0.076	0.080	1.95	2.05	0.076	0.080
F	3.90	4.10	0.154	0.161	3.90	4.10	0.154	0.161
G	7.90	8.10	0.311	0.319	7.90	8.10	0.311	0.319
H	7.40	7.60	0.291	0.299	7.40	7.60	0.291	0.299
ØJ	1.50	1.60	0.059	0.063	1.50	1.60	0.059	0.063
ØK	1.50	1.60	0.059	0.063	1.50	1.60	0.059	0.063
L	3.30	3.5	0.130	0.138	3.30	3.5	0.130	0.138
L_1	1.27	1.47	0.050	0.058	1.27	1.47	0.050	0.058
L_2	0.25	0.35	0.010	0.014	0.25	0.35	0.010	0.014
ΘL	–	45°	–	450	–	45°	–	450
M	1.10	1.30	0.043	0.051	1.10	1.30	0.043	0.051
M_1	1.50	1.70	0.059	0.067	1.50	1.70	0.059	0.067
ØM	–	0.30	–	0.013	–	0.30	–	0.013
R	1.50	2.50	0.059	0.098	1.50	2.50	0.059	0.098
ØN	12.8	13.2	0.504	0.520	12.8	13.2	0.504	0.520
ØP	21.5	22.5	0.847	0.886	21.5	22.5	0.847	0.886
T	1.00	2.00	0.039	0.078	1.00	2.00	0.039	0.078
V	53.0	54.0	2.087	2.126	53.0	54.0	2.087	2.126
W	16.4	18.4	0.646	0.724	16.4	18.4	0.646	0.724

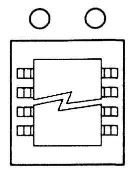
Tape and Reel Options for SO-8 and SO-16





SECTION A-A





Package Orientation

Quantity Per Reel	
SO-8	2500
SO-16	2500

	SO-8				SO-16			
	Millimeters		Inches		Millimeters		Inches	
Dim	Min	Max	Min	Max	Min	Max	Min	Max
A	11.9	12.1	0.469	0.476	15.9	16.1	0.626	0.634
B	1.65	1.85	0.065	0.073	1.65	1.85	0.065	0.073
C	5.10	5.30	0.201	0.209	10.35	10.55	0.407	0.415
D	6.30	6.50	0.248	0.256	6.55	6.75	0.258	0.266
E	7.90	8.60	0.311	0.339	7.90	8.10	0.311	0.319
F	3.90	4.10	0.154	0.161	3.90	4.10	0.154	0.161
G	5.10	5.30	0.200	0.209	10.35	10.55	0.407	0.415
H	0.25	0.35	0.010	0.014	0.25	0.35	0.010	0.014
ØJ	1.50	1.60	0.059	0.063	1.50	1.60	0.060	0.063
K	1.90	2.30	0.075	0.091	1.90	2.30	0.075	0.091
ØK	1.50	1.70	0.059	0.067	1.40	1.60	0.055	0.063
L	328	332	12.91	13.07	328	332	12.91	13.07
ΘL	–	3°	–	3°	–	3°	–	3°
M	1.50	2.50	0.059	0.098	1.50	2.50	0.059	0.098
ØN	12.8	13.2	0.504	0.520	12.8	13.2	0.054	0.520
ØP	21.5	22.5	0.847	0.886	21.5	22.5	0.847	0.886
T	1.00	2.00	0.039	0.078	1.00	2.00	0.039	0.078
V	53.0	54.0	2.087	2.126	53.0	54.0	2.087	2.126
W	12.4	14.4	0.488	2.667	16.4	18.4	0.646	0.724

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JAN Devices
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Reseda
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